Radio Frequency Low Noise and High Q Integrated Filters in Digital CMOS Processes

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Radio Frequency Low Noise and High Q Integrated Filters in Digital CMOS Processes

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Summary

Presented in this work is a novel design technique for CMOS integration of RF high Q integrated filters using positive feedback and current mode approach. Two circuits are designed in this work: a 100MHz low-noise and high Q bandpass filter suited for an FM radio front-end, and a 2.4GHz low-noise and high-Q bandpass filter suited for a Bluetooth front-end. Current-mode approach and positive feedback design techniques are successfully used in the design of both circuits.

The 100MHz tunable low-noise bandpass filter is fabricated through the NSC 0.18um CMOS process. Silicon area of the core circuit is $0.4\,mm^2$. The circuit achieves 3.15uV RF sensitivity with 26dB SNR, and the total current consumption is 12mA. The center frequency of the filter is tunable from 80MHz to 110MHz, and the Q value is tunable from 0.5 to 28.9. 1 dB compression point is measured as -34.0dBm, combined with noise measurement results, a dynamic range of 54.1 dB results.

The 2.4GHz tunable low-noise bandpass filter is also fabricated through the NSC 0.18um CMOS process. Silicon area of the core circuit is $1\,mm^2$. Integrated spiral inductors are developed for this design. Patterned ground shields are laid out to reduce inductor loss through substrate, especially eddy current loss when the circuit is fabricated on epi wafers. Accumulation mode MOS varactors are designed to tune the frequency response. The center frequency of the circuit is tunable from 2.4GHz to 2.5GHz, and the Q value is tunable from 20 to 120. The 1 dB compression dynamic range of the circuit is 50dB.

CHAPTER 1

INTRODUCTION

1.1 Objective and Applications

High performance analog filters are widely used in today's electronic equipment, among which we can find cell phones, radios, digital imaging devices, etc. In the past two decades, continuous efforts have been devoted to the design of analog integrated filters in standard digital CMOS processes, such that low-cost and compact electronic device is resulted. However, discrete filters such as Surface Acoustic Wave (SAW) filters and ceramic filters still play a dominant role as high-Q RF filtering solutions.

High-Q filters are demanded in various applications. For example, at wireless front-end, radio frequency (RF) filters are placed right next to antennas to 'select' the desired signal bands, and RF image rejection filters are placed in between LNAs and mixers to attenuate image signals. Also high-Q filters are desired as intermediate frequency (IF) channel-selection filters in heterodyne receivers. Shown in Figure 1.1 is the architecture of a typical heterodyne wireless receiver, highlighted are off-chip high frequency and high-Q filters.

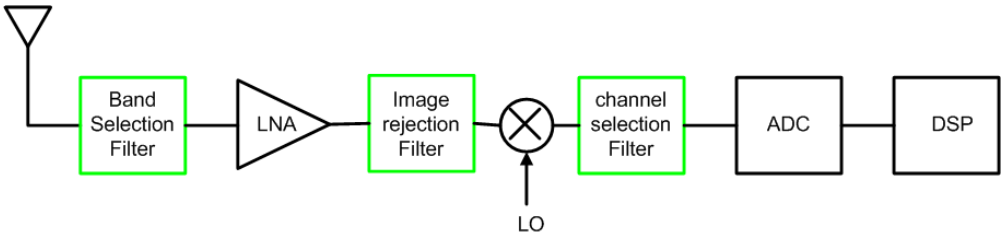
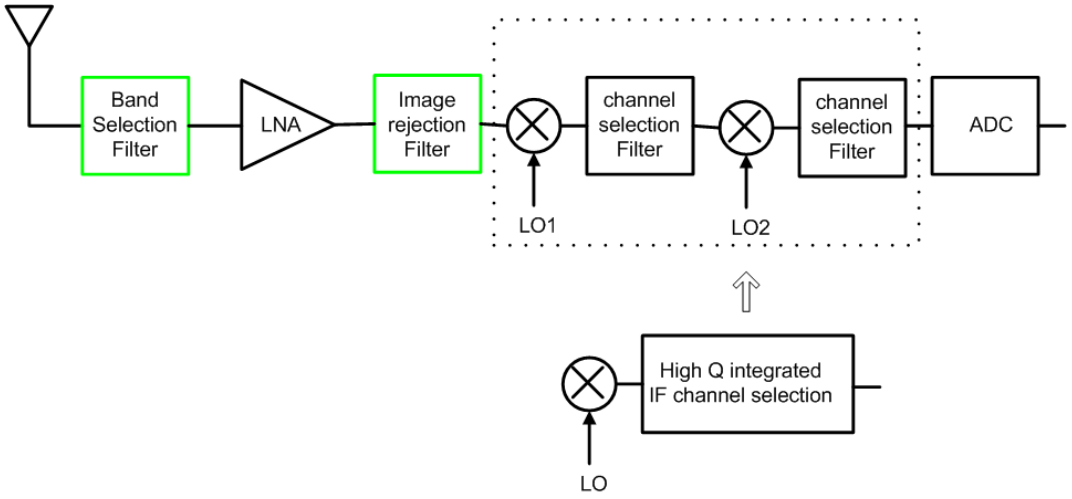


Figure 1.1 Architecture of a typical wireless receiver

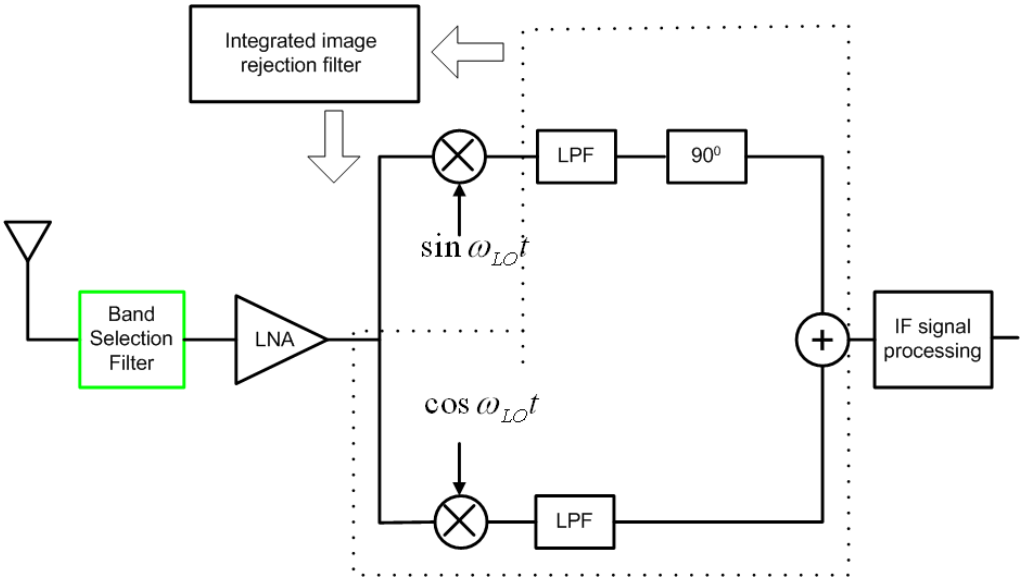
Single-chip receiver architectures have been extensively studied [31, 33]. To circumvent the requirement of high-Q filtering, approaches have been taken to revise the simple heterodyne architecture shown above in Figure 1.1. To name a few, homodyne receivers directly convert RF signals into baseband signals by choosing local oscillator frequency the same as RF, remove IF filters and achieve channel selection using digital filters; image rejection receivers make 'duplicated' signal path, where images are negated and finally cancelled by summing up signals from two paths; Dual-IF receivers [55] have been built to break the channel selection filtering into two parts, and perform partial channel selection at progressively lower center frequencies, such that requirements of high Q are relaxed at each stage. Architectures of above mentioned receivers make signal chip solutions feasible, however, on the other hand, they all, in some way, suffer from loss of performance.

In a homodyne receiver, since incoming signals are directly downconverted to baseband, self-mixing of LO signals with LO leakage through LNA generate extraneous DC offsets; flicker noise substantially corrupt signals in a heterodyne receiver since all of the signal processing is done at baseband; also heterodyne receivers suffer from even-order distortions which otherwise can be avoided if heterodyne architectures are taken.

Image rejection receivers and Dual IF receivers trade the system complexity with the need of high Q filtering. Integration of RF and IF high Q filters help to simply the design of such receivers, for example, to remove one of the two sets of IF circuitry from Dual IF receivers (Figure 1.2 (a)) or one of the quadrature signal paths from a image rejection receiver (Figure 1.2 (b)). Objective of this work is to investigate the design of integrated RF filters suitable for various wireless RF applications.



(a)



(b)

Figure 1.2 (a) A Dual IF receiver (b) An image rejection receiver

1.2 Design Bottlenecks

It's interesting to see that discrete components inside a wireless receiver are used to perform RF and IF filtering and impedance matching. Design of RF and IF filters becomes a bottleneck in the design of integrated wireless receivers. Reasons lie in the following facts: design trade-offs and requirements of high performance on-chip passive elements.

Illustrated in Figure 1.3 are general performance parameters to be optimized in most analog IC designs. It is commonly agreed that performance tradeoffs are through out analog IC designs especially when RF circuits need to process signals with large dynamic range [11-12, 20]. The situation is exacerbated in case of high Q RF filter designs especially when the design has to be done under the constraint of limited amount of power and supply voltage [20].

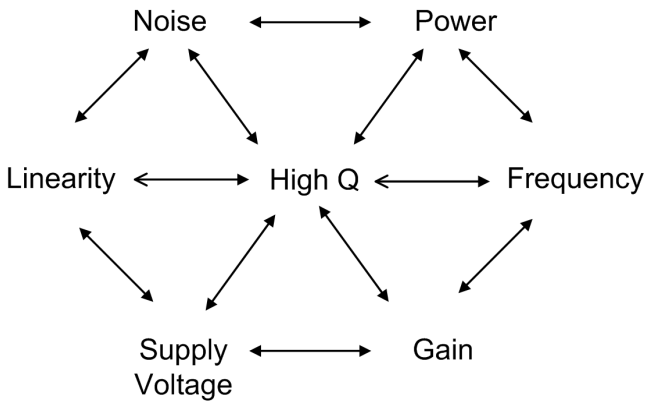


Figure 1.3 RF design hexagon for high-Q filters

On-chip passive elements including inductors and capacitors are required for most of RF filters and amplifiers. It's proven that Q of RF filters are directly related to the Q value of tank inductors [45]. High Q passive elements greatly ease the design of high Q RF filters. However, in most CMOS processes, the Q value of inductors are limited to the range of 3~6 due to thin metal layers, limited silicon space, parasitic capacitance to substrate and eddy current loss through substrate. Extensive studies have been carried out to optimize designs of on-chip inductors [46-49].

Extra precautions need to be taken when laying out RF high Q filters. At gigahertz frequencies, resistance and parasitic capacitance associate with metal wires have significant effects on system performance. As a result, more design iterations are necessary to ensure a proper implementation (Figure 1.4).

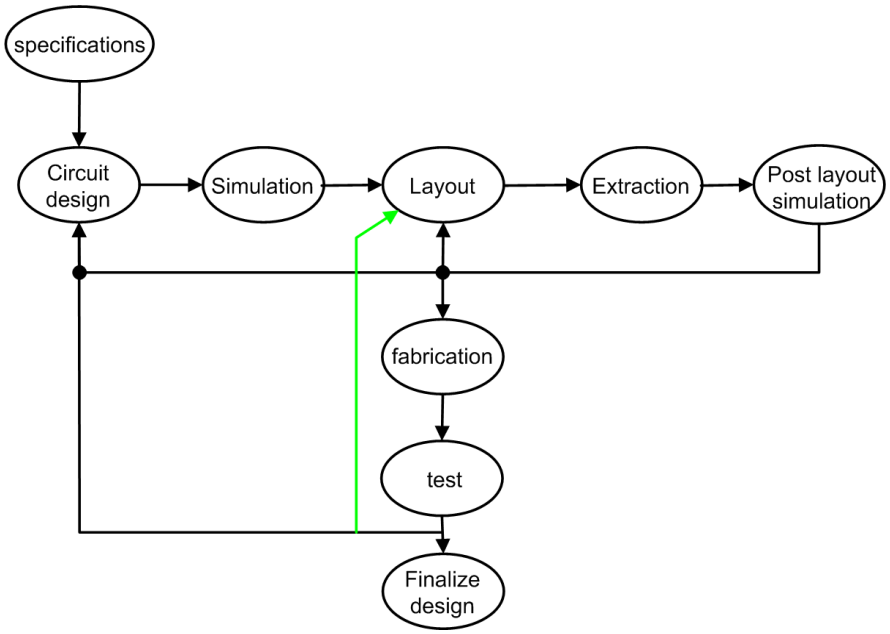
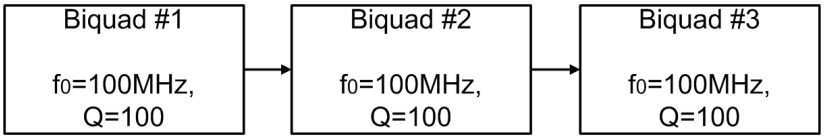
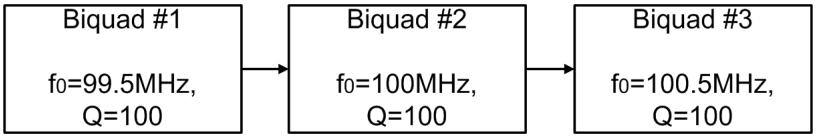


Figure 1.4 RF circuit design procedures

Compared to other RF circuits in CMOS process, layout of high Q filters requires more accurate matching concerning ratios of component parameters [57]. An example is illustrated in figure 1.5. A 100MHz Q=198 bandpass filter is built by cascading three second-order stages (biquads), each of the three biquads is designed to have Q=100, gain=0dB, and resonant at 100MHz, as shown in Figure 1.5(a). Assume the resonant frequency of each biquad is determined by ratio of transconductance, g_m, and load capacitance, C. Ideally, the load capacitance for all three biquads should be identical such that they all resonant at the same frequency. Now assume 0.5% mismatch in capacitors layout, which makes the resonant frequency of the first biquad become 99.5MHz, and that of the third biquad 100.5MHz, as shown in Figure 1.5(b). From the simulation result in figure 1.5(c), we can tell that Q of the system in Figure 1.5(b) is 117 and there is 6dB loss at the resonant frequency, compared to the result from system in Figure 1.5(a), there is a 41% error in Q value. Note that a 0.5% mismatch in capacitance ratios results in more than 40 percent change in Q value.



(a)



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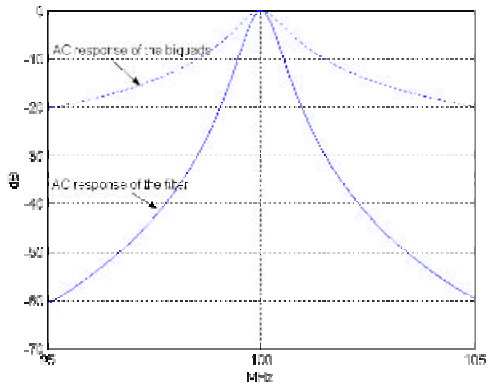
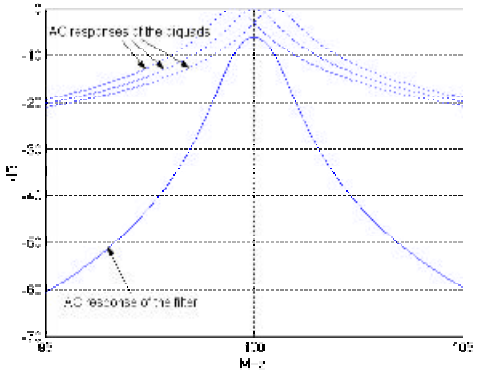


(c)



(d)

Figure 1.5 (a) Cascade three identical biquads; (b) cascade biquads when there is 0.5% error in capacitor matching; (c) AC response of (a); (d) AC response of (b)

1.3 This Work

This work is concentrated on the design of RF integrated low-noise and high-Q bandpass filters in digital CMOS processes. Two circuits are developed in this work. The first circuit is a 100MHz low-noise (RF sensitivity =3.15uV) and high Q (Q=29) bandpass filter to be used in a FM radio front-end, and the second one is a 2.4GHz low-noise and high Q bandpass filter for Bluetooth receivers. This thesis consists of the following parts. Both feature high Q and low noise, and are suitable for various RF applications.

A brief review of integrated filters that are capable of achieving high Q at high frequency is given in chapter 2. Advantages and disadvantages of passive filters, active-RC filters using opamps, switch capacitor filters, gm-C filters, and Q-enhanced LC filters are discussed in chapter 2.

Discussions on system architectures are carried out in chapter 3. The two circuits designed in this work share the same topology architecture at system level. The basic idea of Q-enhancement is achieved by using positive feedback. System level performance analysis is also given in chapter 3.

Details design of 100MHz and 2.4GHz circuits are described in chapter 4 and 5, respectively. Included in chapter 4 and 5 are schematic circuits, simulation results, practical design considerations, layouts, test setup, and measurement results.

A summary of this work is given in chapter 6, also future work and possible improvements to current research are proposed.

CHAPTER 2

HIGH FREQUENCY AND HIGH Q

INTEGRATED FILTERS

In this chapter, high frequency and high Q integrated filters reported in literature in the past two decades are reviewed. Critical design issues are discussed concerning Q, noise, linearity, and dynamic range. The following types of filters are covered in this chapter: passive filter, active-RC filter, MOSFET-C filter; Gm-C filter, and Q-enhanced LC filter.

2.1 Passive Filters

Passive filters are built based on RLC passive elements, and they have played important roles in the history of analog filters [58]. Many filter functions were originally implemented using RC networks or LC ladders, the latter is proved to have lower sensitivity to component variations [54, 58]. A lot of active filters are developed based on implementing inductors/resistors in their passive prototypes by active means. For example, active-RC filters are obtained if inductors in a LC ladder filter are replaced by

opamps and resistors; Gm-C filters result by replacing the inductors with transconductance and capacitors.

Passive filters have many advantages in terms of linearity, dynamic range and power. Due to the linear nature of passive components, passive filters operate over a large range of input power. Active filters fall out of their linear operation range when bias transistors are unable to provide enough dynamic current, or when voltages are clipped by power supplies. Passive filters don't experience such problems. Since there are no active elements, nonlinearity due to current saturation is avoided; furthermore, since passive filters are input-driven, power supply limitation no longer exists.

Passive filters offer good noise performance due to the absence of noisy transistors. Ideally, inductors and capacitors are noiseless. Major noise sources in passive filters are thermal noise from resistors. Passive filters can achieve excellent dynamic ranges that outweigh all active filters.

As mentioned above, passive filters are input-driven, which imply that there is no need to dc bias passive filters thus dc power supply is not needed. Passive filters can work at very high frequencies up to several hundreds of MHz, with parasitic capacitance being the primary limitation.

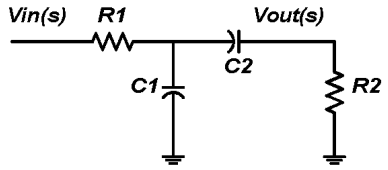


Figure 2.1 A second-order passive bandpass filter

Although passive filters have superior performance in terms of dynamic range and power, they are not frequently used in today's applications. A lot of active filters adopt structures of passive RLC network, and use active means to compensate for the drawbacks of passive filters, which include:

- Pass band loss

An example of a second-order passive filter is shown in Figure 2.1. The transfer function of the filter is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{R_1C_1}}{\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2}} \cdot \frac{s\cdot(\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2})}{s^2+s\cdot(\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2})+\frac{1}{R_1R_2C_1C_2}} \quad (2.1)$$

From (2.1), we can see that the mid-band gain of the filter is determined by:

$$A = \frac{\frac{1}{R_1C_1}}{\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2}} \quad (2.2)$$

Let $r = R_1/R_2$ and $\gamma = C_1/C_2$, we can rewrite (2.2) as:

$$A = \frac{1}{1+\rho\gamma+\rho} \quad (2.3)$$

Since $\rho > 0$ and $\gamma > 0$, $1+\rho\gamma+\rho > 1$, therefore we can draw a conclusion that the mid-band gain, A, is always less than 1. This can also be explained from the energy point of view. Since energy can only be introduced into a system using active components, a passive filter always has a gain of less than 0dB.

- Large silicon area

It takes a lot of area to integrate passive components in CMOS processes. Resistors in CMOS processes are usually implemented in one of the following forms: poly resistors; metal resistors; or MOS resistors. A typical value of sheet resistance of a polysilicon layer is approximately $8\Omega/square$, and metal layers usually have much smaller sheet resistance as approximately $100m\Omega/square$. MOS resistors have larger values of sheet resistance, however, the linearity performance is much worse since the input voltage must be limited to keep the MOSFET operating in proper region. There are several ways to build capacitors in CMOS processes. Poly-Poly capacitors have the best linearity performance and thus are most frequently used. Unit capacitance of typical poly-poly capacitors is approximately $1fF/um^2$. Theoretically it takes approximately $40um$ by $40um$ to build a 1pF capacitor. In practice, much larger areas are required to layout capacitor arrays for best matching. Parasitic capacitance associated with bottom plane of poly-poly capacitance can be up to 20% of the designed capacitance value. Flux capacitors are built using metal layers, they have very low parasitic of approximately 1%. However, unit capacitance of flux capacitance is much smaller, which makes building a capacitor of several tens of pFs much more difficult. MOS capacitors are designed for tuning. Like a MOS resistors, a MOS capacitor has worse linearity resistance compared to poly-poly or flux capacitors. A lot of efforts have been devoted to the integration of inductors in CMOS processes [46-47, 59-61]. Inductors are usually implemented using spiral structure. A significant amount of area is required for spiral inductors with a value of several nHs, especially when a thick trace width is required to minimize the value of series resistance.

- Tuning

Values of passive components change significantly due to temperature and process variations. For example, capacitance of poly-poly capacitors may vary over $\pm 20\%$ of the designed capacitance, and resistance of MOS resistors may change $\pm 20\%$ as temperature varies from $30^{\circ}F$ to $110^{\circ}F$.

Tuning of integrated passive filters is implemented by varying the values of passive components. Control of passive elements is much more difficult than that of transistors, whose properties are easily varied by adjusting dc bias currents. One way of discretely controlling the value of passives is to build switched arrays. Ideally, switches provide perfect connection when closed and infinite resistance when opened. However, integrated switches usually have hundreds ohms of resistance when closed, this resistance may cause a lot of loss in both resistor arrays and capacitor arrays.

- Lack of accurate models

It's difficult for the models of integrated passive components to be as accurate as their discrete counterparts. Modeling of on-chip passive elements is very complicated and involves a lot of parameters. For example, modeling of on-chip inductors has been an active research area for the past decade [45-49].

2.2 Active-RC Filters

At frequencies below hundreds of kilohertz, sizes of available on-chip inductors are generally too large to allow any practical designs of integrated inductors. Also it's not economical to design gm-C filters at this frequency range due to the large size of capacitors. Active-RC filters based on OPAMPs are widely used for applications in these frequencies.

General structure of active-RC filters can be developed from passive RC network [54], as illustrated in Figure 2.2. The passive network is a n-node RC network, feedback from the output of the RC network is applied to input/internal nodes of the RC network, feedback gains are set by K_{01}, K_{02}, … and K_{0n}. The input gains are controlled by K_{11}, K_{12},…, and K_{1n}. The two sets of gains, K_{01}, K_{02}, … and K_{0n}, and K_{11}, K_{12}, … and K_{1n}, are realized by active means.

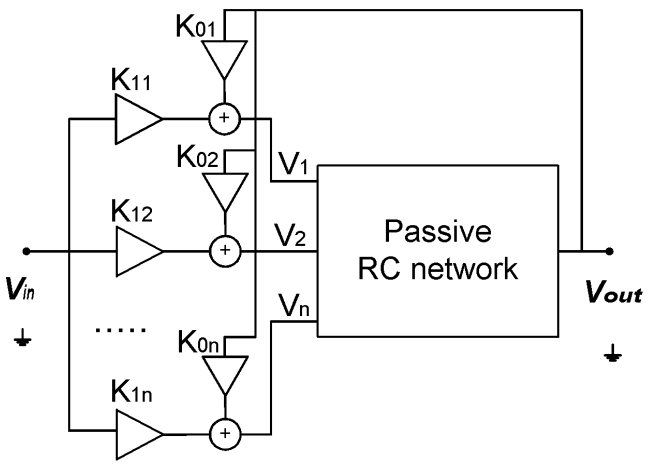


Figure 2.2 A general structure of active-RC filters [54]

Assume the transfer function of the passive RC network is defined as:

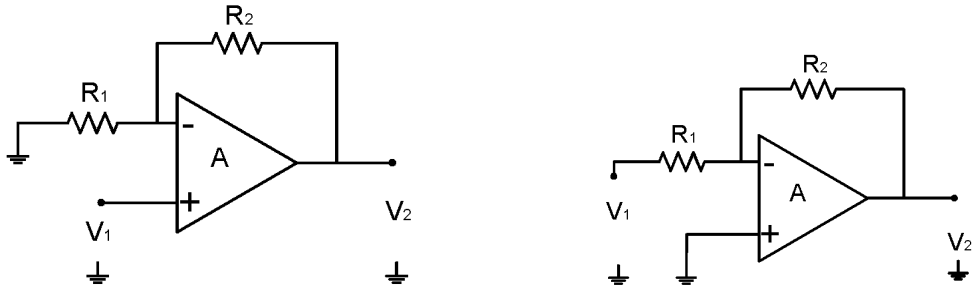
$$V_{out\_Passive\_RC}(s) = \frac{N_1(s)\cdot V_1(s) + N_2(s)\cdot V_2(s) + \cdots\cdots + N_n(s)\cdot V_n(s)}{D(s)} \qquad (2.5)$$

The overall transfer function of the system shown in Figure2.2 can be expressed as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{K_{11}N_1(s) + K_{12}N_2(s) + \cdots\cdots + K_{1n}N_n(s)}{D(s) - K_{01}N_1(s) - K_{02}N_2(s) - \cdots\cdots - K_{0n}N_n(s)} \qquad (2.6)$$

Assume K_{01}, K_{02}, … and K_{0n}, and K_{11}, K_{12}, … and K_{1n} are ideal amplifiers which have infinite bandwidth, we can manage to place the poles and zeros of H(s) anywhere on the complex plane if an appropriate passive RC network is chosen. Generally speaking, any form of a transfer function that can be realized by a RLC network can be implemented using the system shown in Figure 2.2 [54].

In active-RC filters designed using OPAMPs, positive or negative gains K_{01}, K_{02}, … and K_{0n}, and K_{11}, K_{12}, … and K_{1n} are implemented by inverting or non-inverting amplifiers based on OPAMPs. Examples of such amplifiers are shown in Figure 2.3.



(a) (b)

Figure 2.3 Amplifiers designed based on opamps (a) A non-inverting amplifier (b) An inverting amplifier

In general, at most four opamps are required to realize the system shown in Figure 2.2, regardless of structures of passive RC networks. A maximum of two opamps are required for implementing each set of gains K_{1i} and K_{0i}, with one configured as non-inverting for positive gains and the other as inverting for negative gains.

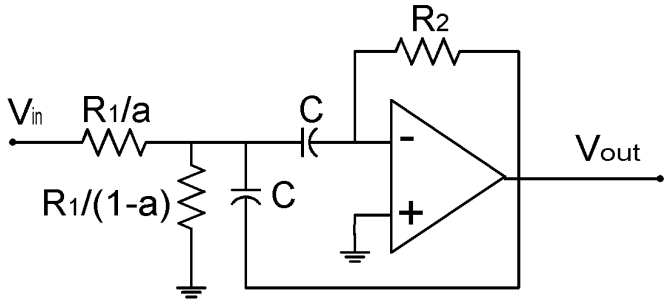


Figure 2.4 A second-order active-RC bandpass filter

As an example, a second-order active-RC bandpass filter is shown in Figure 2.4. Assume the OPAMP is ideal, transfer function of the filter shown in Figure 2.4 can be expressed as:

$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{-as\dfrac{1}{R_1C}}{s^2+s\dfrac{2}{R_2C}+\dfrac{1}{R_1R_2C^2}} \tag{2.7}$$

If we rewrite (2.7) in the standard form with center frequency ω_0 and quality factor Q, we can identify the filter parameters as

$$\omega_0=\sqrt{\frac{1}{R_1R_2}}\frac{1}{C} \qquad Q=\frac{1}{2}\sqrt{\frac{R_1}{R_2}} \tag{2.8}$$

$$mid-band\_gain=\frac{1}{2}a\frac{R_2}{R_1}$$

Performance of active-RC filters suffer from non-idealities of OPAMPs. Effects of finite gain-bandwidth of OPAMPs on the performance of active-RC filters have been discussed in literature [54].

2.3 MOSFET-C Filters

As mentioned earlier, on-chip metal or poly resistors occupy a lot of silicon space and the resistance values are hard to control, making the tuning difficult. MOSFET-C filters are a solution to compact and tunable filters at low frequencies especially at audio frequencies.

It is well known that if a MOS transistor is biased in triode region, and $V_{DS} << 2(V_{GS} - V_T)$, the drain current i_D is a linear function of V_{DS}. This implies that a MOSFET can operate as a linear resistor, as shown in Figure 2.6. The resistance value can be written as:

$$r = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_T)} \tag{2.9}$$

where V_T is the threshold voltage of the transistor, W and L are channel width and length of the transistor, μ_n is carrier mobility and C_{OX} is the oxide capacitance per unit area [52, 53]. Equation (2.9) indicates that the resistance value of a MOSFET resistor is controlled by the gate-source voltage V_{GS}.

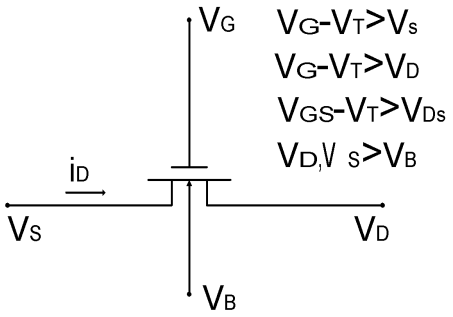


Figure 2.5 A MOSFET resistor

If we replace resistors in the filter shown in Figure 2.4 with MOSFET resistors, a MOSFET-C filter as shown in Figure 2.6 results. As we can see, resistance values of all resistors are controlled by the control voltage V_{ctrl}, and ratios of resistance are determined by ratios of (w/L)'s of transistors. This implies that good matching between transistors is required to ensure the accuracy of resistor ratios and thus the accuracy of frequency response. When layout MOSFET-C filters, transistor arrays may be necessary to achieve desired matching accuracy.

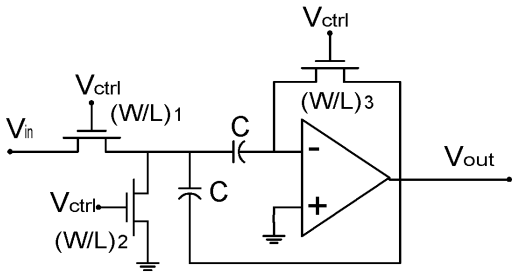


Figure 2.6 A MOSFET-C filter

As in active-RC filters, OPAMPs are key building blocks in MOSFET-C filters. OPAMP nonidealities have similar effects on performance of MOSFET-C filters as they

do on active-RC filters. MOSFET-C filters are not suitable for high frequency applications due to finite gain-bandwidth of OPAMPs.

In general, linearity of MOSFET-C filters is worse than other filters that use poly or metal resistors. This is because the linearity of MOSFET-C filters depends on the linearity of MOS resistors, and MOS resistors have bad linearity performance due to the nonlinear nature of MOS transistors. A fully balanced MOSFET-C filter with differential inputs and outputs improves the linearity since second-order harmonic is suppressed by the differential structure [18].

To make MOSFET-C filters operate properly, signals must be small enough such that MOS transistors work in triode region, and the linear relationship described in equation (2.9) is valid. This limits signal swing that MOSFET-C filters can handle.

2.4 Gm-C Filters

Gm-C filters, also named OTA-C filters or transconductance-C filters are widely used in high frequency applications range from several megahertz to hundreds of megahertz. Gm-C filters are designed using an operational transconductance amplifier (OTA), and capacitors.

Compared to active-RC filters, Gm-C filters use OTAs instead of opamps to overcome effects of opamp nonidealities on active-RC filters. Also, OTAs have the advantages of easy tunability and generally simpler circuitry than most opamps. An OTA is a voltage controlled current source as shown in Figure 2.7, it is tunable through varying DC bias current. Properties of OTAs have been extensively studied in the past two

decades, and many OTAs with very good linearity and superior high frequency performance have been designed [13-18].

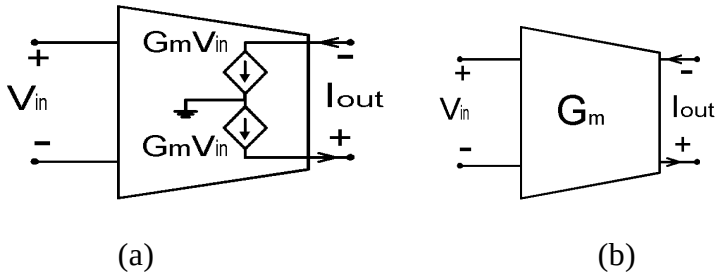


Figure 2.7 (a) block diagram of a transconductor (b) symbol of (a)

Performance of Gm-C filters is mainly determined by OTAs. An ideal OTA is a voltage controlled current source, with constant transconductance value, Gm, over infinite bandwidth, and infinite input and output impedance. However, practical designs of OTAs in CMOS processes exhibit nonidealities. For example, channel resistances associated with MOS transistors, r_{ds}, are finite value which are typically hundreds of kilo-ohms to several mega-ohms; parasitic capacitance associated with poly gates and metal paths generate unwanted poles/zeros which limit the performance of high frequency and high Q gm-C filters, also parasitic poles/zeros might jeopardize stability of overall systems when such OTAs are used in high frequency and high Q applications [7, 8].

2.4.1 Gm-C Integrators

Nonidealities of OTAs are usually evaluated by 'excess phase shift' of Gm-C integrators. A Gm-C integrator is shown in Figure 2.8(a). Resonant frequency of the

integrator is expressed as $w_0 = \frac{G_m}{C}$. Figure 2.8(c) shows amplitude and phase response of Gm-C integrators over frequency. Note that integrators built using ideal OTAs exhibit 90 degree phase shift and 0dB attenuation at w_0. OTA nonidealities make the phase shift at resonant frequency deviated from 90 degree, the deviation is defined as 'excess phase shift'. Amount of excess phase shift reflects the amount of effects OTA nonidealities may have on the performance of gm-C filters. Assuming the transfer function of the OTA shown in figure 2.8(b) is:

$$Gm(s) = Gm_0 \frac{1 + \frac{s}{w_z}}{1 + \frac{s}{w_p}} \tag{2.10}$$

where w_z and w_p are dominant zero and pole frequencies, respectively. Gm_0 is the DC transconductance. R_0 and C_0 are parasitic resistance and capacitance associated with output terminals, respectively. Thus the transfer function of Gm-C integrators built using nonideal OTAs can be written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{Gm_0 R_0}{1 + sR_0(C + C_0)} \cdot \frac{1 + \frac{s}{w_z}}{1 + \frac{s}{w_p}} \tag{2.11}$$

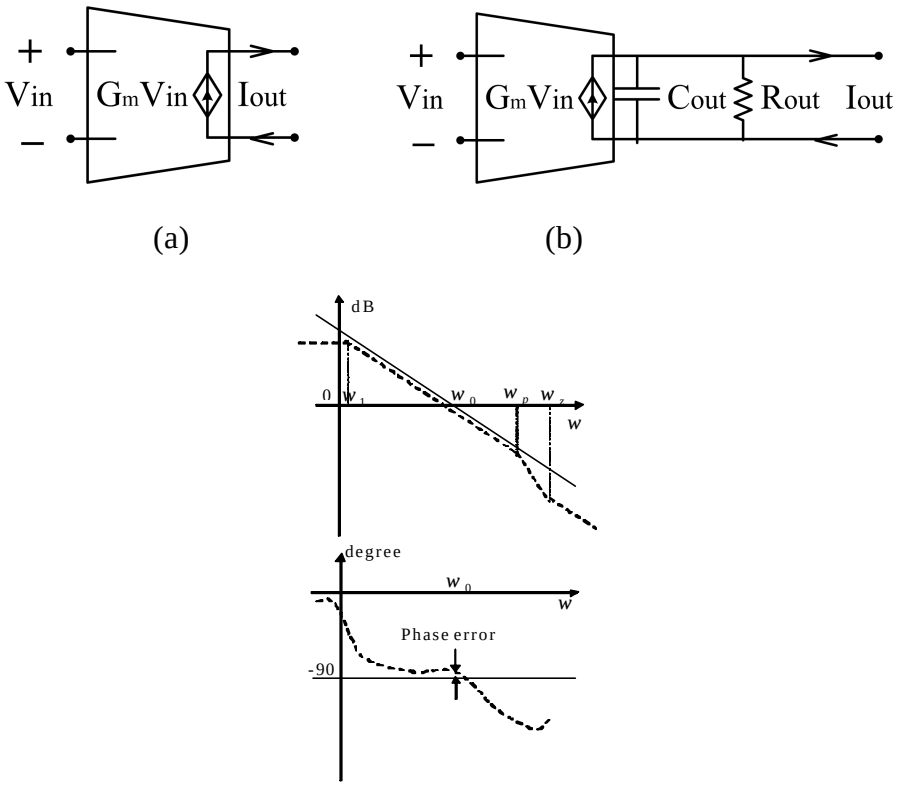


Figure 2.8 (a) a gm-C integrator (b) an nonideal OTA
(c) frequency responses of ideal and nonideal Gm-C integrators
(solid lines—ideal integrator, dotted lines—nonideal integrator)

High Q Gm-C integrators are key elements in the design of high Q Gm-C biquads. It is mathematically prove that for high-Q integrators, Q is approximately inversely proportional to excess phase shift q_p [8].

$$\frac{1}{Q_{\text{int}eg}} \approx q_p \tag{2.12}$$

From (2.11), the phase response at unity gain frequency can be written as:

$$\arg[A(jw)] = -\tan^{-1}(G_{m0}R_0) + \tan^{-1}(\frac{w_0}{w_z}) - \tan^{-1}(\frac{w_0}{w_p}) \tag{2.13}$$

If $G_{m0}R_0 >> 1$ and $w_z, w_p >> w_0$, (2.6) can be simplified as follows:

$$\arg[A(jw)] \approx -\frac{p}{2} + \frac{1}{G_{m0}R_0} + \frac{w_0}{w_z} - \frac{w_0}{w_p} \tag{2.14}$$

Since the ideal integrator frequency response is −90°, the phase error of the integrator frequency response at unity gain frequency is:

$$q_p = \frac{1}{G_{m0}R_0} + \frac{w_0}{w_z} - \frac{w_0}{w_p} \tag{2.15}$$

If we consider high order zeros and poles of a transconductor, a general expression for phase error of Gm-C integrators can be written as:

$$\frac{1}{Q_{\text{int}eg}} \approx q_p = \frac{1}{G_{m0}R_0} + w_0\left(\sum_{i=0}^{\infty}\frac{1}{w_{z_i}} - \sum_{j=0}^{\infty}\frac{1}{w_{p_j}}\right) \tag{2.16}$$

Several very important facts can be observed from (2.16). First we can see that the phase error consists of two parts. One part is the phase lead caused by finite DC gain of Gm-C integrators which in turn is caused by finite output impedance, and the other part is the excess phase caused by parasitic poles and zeros as expressed in the second term of (2.16). **Therefore, the Q value of a Gm-C integrator can be**

increased either by increasing R_0 or increasing parasitic poles/zeros frequencies. The second fact we note from (2.16) is that the amount of excess phase increases when the unity gain frequency increases. This explains why it is more difficult to build high Q filters at high frequencies than at low frequencies.

It is desirable for terms in (2.16) to cancel with each other. However, it may not be practical in the design of real filters. To reduce phase errors and increase Q of Gm-C integrators, special care has to be taken in increasing either R_0 and/or parasitic poles/zeros frequencies.

2.4.2 Gm-C Biquads

Construction of high order Gm-C filters is based on topology of passive RLC networks, realization of resistors using transconductors, and emulation of inductors using Gm-C gyrators. An example of second order Gm-C filters is shown as follows (Figure 2.9).

Shown in Figure 2.9(a) is a second-order RLC prototype filter; illustrated in Figure 2.9(b) is a transformation is taken at the input of circuit in Figure 2.9(a); Figure 2.9(c) shows an example of implementing resistors using transconductors; Figure 2.9(d) shows a gm-C realization of inductors; Finally, in Figure 2.9(e), a gm-C biquad is built based on the prototype filter shown in Figure 2.9(a), and with all passive components replaced by their gm-C realizations.

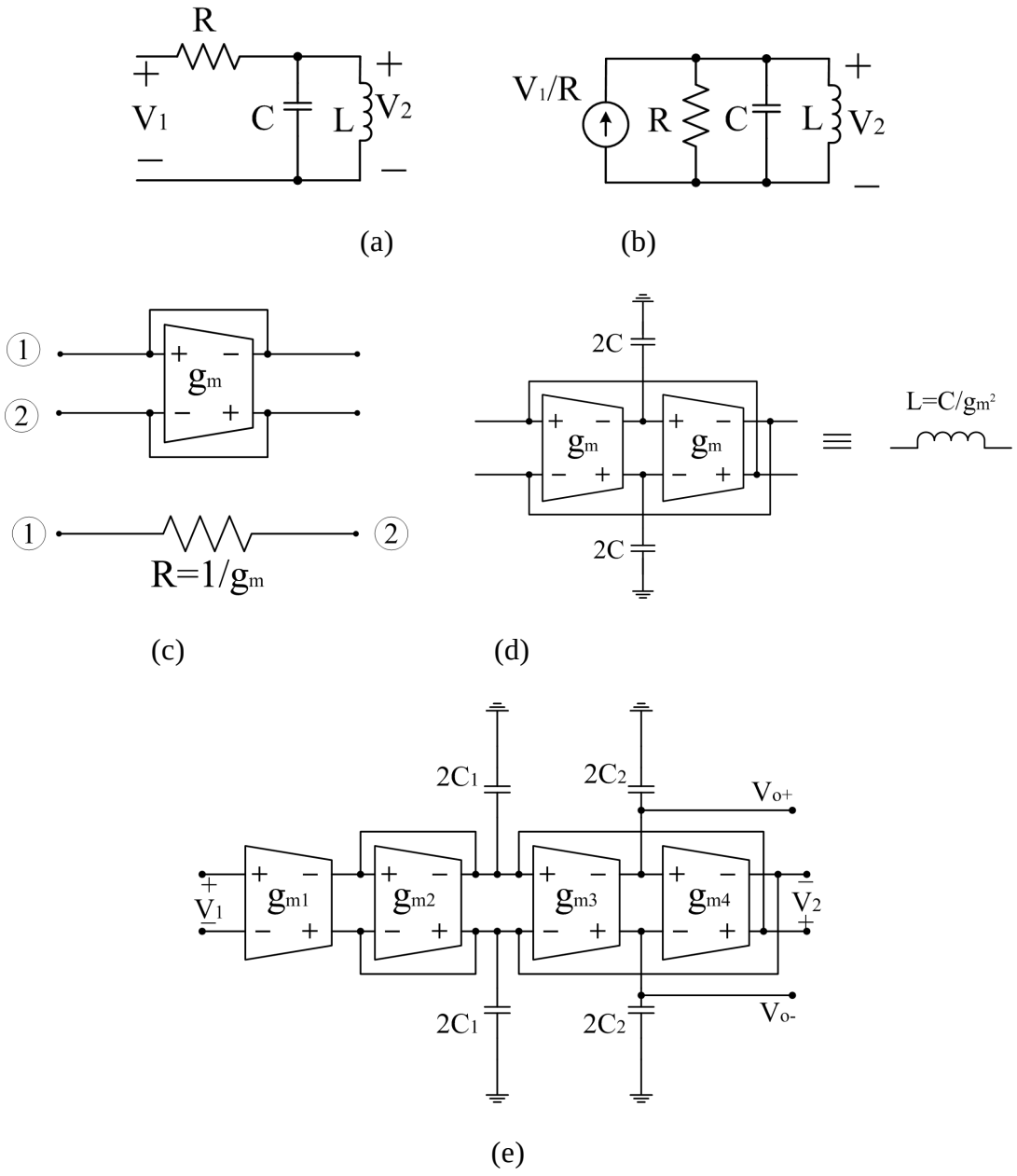


Figure 2.9 (a) passive RLC prototype; (b) input transformation of (a); (c) realization of resistors (d) emulation of differential grounded inductors (e) a second order gm-C filter

Assuming all transconductors are ideal, the transfer function of the gm-C filter shown in Figure 2.9(e) can be written as:

$$\frac{V_2(s)}{V_1(s)} = \frac{s\frac{g_{m1}}{C_1}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{2.17}$$

A lowpass biquad is also obtained from V_1 to Vo.

$$\frac{V_o(s)}{V_1(s)} = \frac{\frac{g_{m1}g_{m4}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{2.18}$$

To investigate the effects of transconductor nonidealities on the biquad, denote output capacitance and conductance of each individual transconductor by C_{out} and g_{out}, respectively. Similarly assume the input capacitance is C_{in}. For simplicity of discussion, values of capacitance and conductance are assumed to be the same for all transconductors.

Rewrite the characteristic equation, we obtain:

$$s^2C_1C_2 + sC_2g_{m2} + g_{m3}g_{m4} \tag{2.19}$$

A straight forward analysis is done by looking into the impedance at each node with the presence of C_{in}, C_{out} and g_{out}. The overall impedance seen at the output of g_{m2} is a function of C_1, C_{out}, C_{in}, and g_{out}. Similarly we can easily find out that the overall impedance seen at the output of g_{m2} is a function of C_2, C_{out}, C_{in}, and g_{out}.

A modified characteristic equation including effects of C_{in}, C_{out} and g_{out} is obtained by:

$$\begin{aligned} sC_1 &\rightarrow s(C_1 + 3C_{out} + 2C_{in}) + 3g_{out} \\ sC_2 &\rightarrow s(C_1 + C_{out} + C_{in}) + g_{out} \end{aligned} \tag{2.20}$$

Substitute (2.20) in (2.19), we obtain:

$$\begin{aligned} & s^2(C_1C_2 + 3C_{out}^2 + 2C_{in}^2 + 3C_{out}C_2 + 2C_{in}C_2 + C_{out}C_1 + C_{in}C_1 + 5C_{out}C_{in}) \\ & + s(g_{m2}C_2 + g_{m2}C_{out} + g_{m2}C_{in} + g_{out}C_1 + 6g_{out}C_{out} + 5g_{out}C_{in} + 3g_{out}C_2) \\ & + g_{m3}g_{m4} + g_{m2}g_{out} + 3g_{out}^2 \end{aligned} \tag{2.21}$$

Assume $g_{m1,2,3,4}$>>gout, $C_{1,2}$>>Cout. Rewrite (2.21), we get:

$$\begin{aligned} & s^2(C_1C_2 + +3C_{out}C_2 + 2C_{in}C_2 + C_{out}C_1 + C_{in}C_1) \\ & + s(g_{m2}C_2 + g_{m2}C_{out} + g_{m2}C_{in} + g_{out}C_1 + 3g_{out}C_2) + g_{m3}g_{m4} + g_{m2}g_{out} + 3g_{out}^2 \end{aligned} \tag{2.22}$$

As can be seen from above equations, Q of the biquad is reduced due to the existence of g_{out}. For high-Q applications, coefficient of the second term in (2.22) becomes very small, and effect of non-zero g_{out}'s becomes dominant. To build high-Q gm-C biquads, g_{out} must be reduced using techniques such as cascoding transistors, or negative resistance [13-19].

This coincides with the analysis of Gm-C integrators, and the conclusion is: to build high Q gm-C filters at RF frequencies, high performance transconductors with small parasitic capacitance and very large output resistance must be built.

2.4.3 Increasing Output Resistance of Transconductors

There are two commonly used techniques to increase output resistance of a transconductor: 'cascoding transistors' approach, and 'negative resistance' approach.

The basic idea of cascode approach is illustrated in figure 2.10. M3 and M2 are inserted in the signal path, and thus enhanced the output resistance by $g_{m3}r_{o3}$ times when compared to a single transistor common source stage. The idea was employed in numerous applications especially when the supply voltage is reasonable large such that the two 'extra' transistors wouldn't jeopardize magnitude of signal swings.

Modifications to the cascode structure shown in Figure 2.10 make the approach feasible for low voltage applications. Folded-cascode circuits [52, 56] have been widely used in low supply voltage applications. Wide-swing cascode circuits [52, 56] are adopted in this work to achieve large voltage swings while the supply voltage is kept at 1.5v.

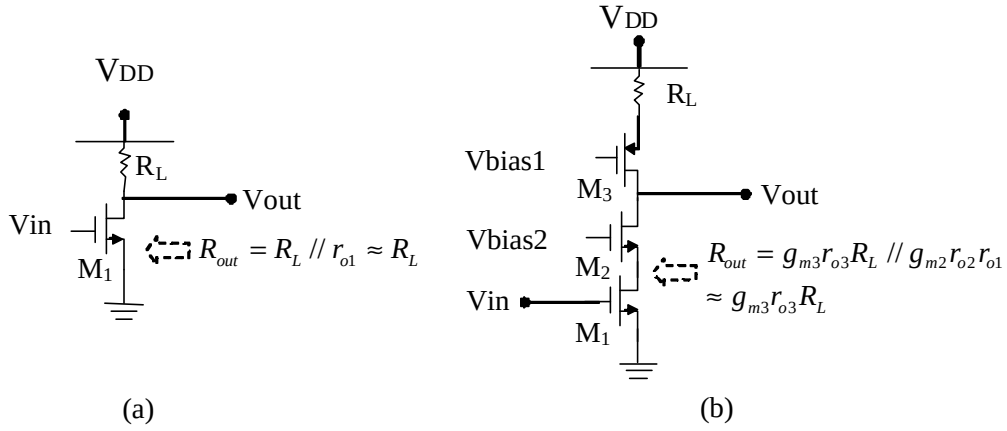


Figure 2.10 Using cascode approach to increase output resistance

The idea of compensating for the effect of low output resistance using negative resistance is explained below in figure 2.11. A transconductor gm2 is cross-coupled and loaded at the output of gm1, to which the output resistance is to be compensated for. If a best estimate on the value of rout is made, we can design

$$\frac{1}{g_{m2}} = r_{out1} // r_{out2} \tag{2.23}$$

such that the overall resistance seen at the output of gm1 is infinite. In reality, the negative resistance value is designed to be very close to but smaller than rout to prevent instability due to over compensation.

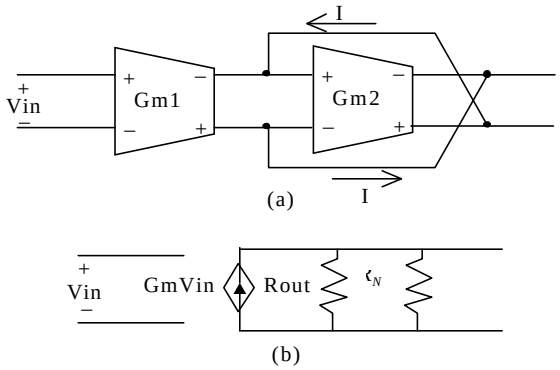


Figure 2.11 Basic concept of negative resistance

An example of a transconductor with negative resistance load (NRL) is given in Figure 2.12.

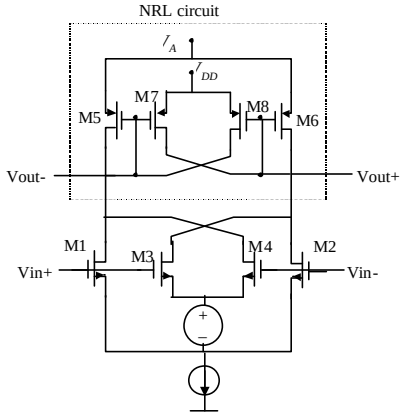


Figure 2.12 A transconductor with NRL.

2.4.4 Linearization of Transconductors

Linear operation of transconductors is only valid when input signal levels are small, and all conditions for MOSFET small-signal analysis are satisfied. When large input signals are applied to transconductors, linear approximation is no longer valid.

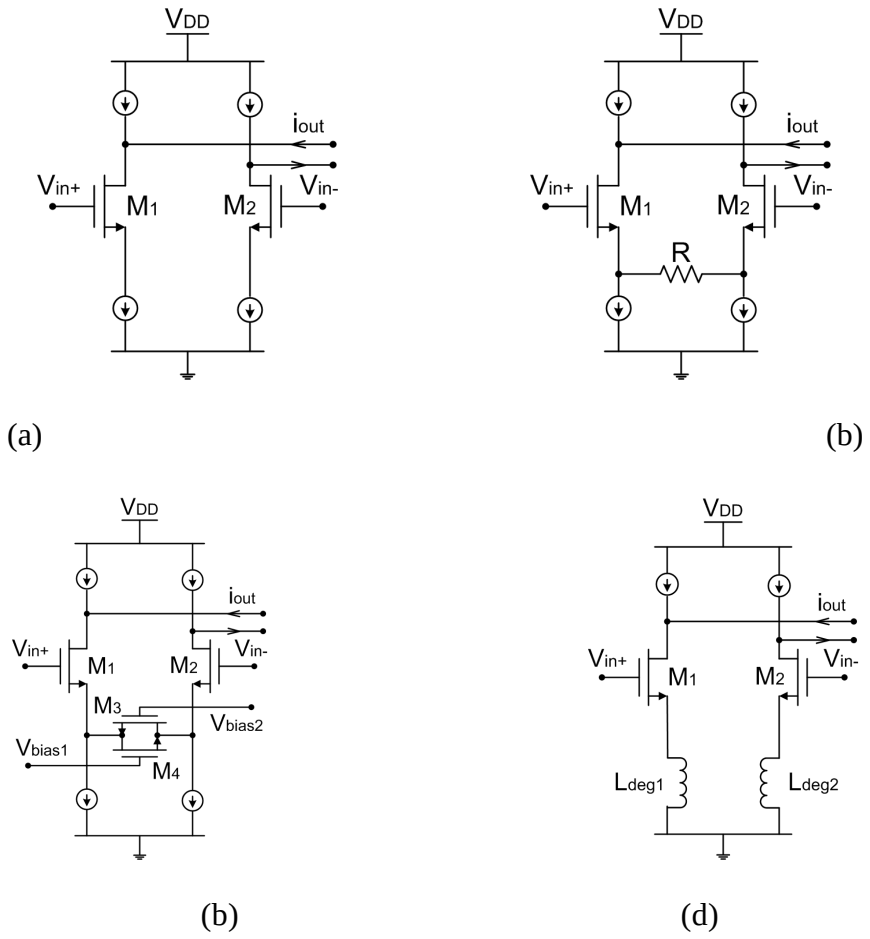


Figure 2.13 Linearization of transconductors (a) a simple differential pair; (b) resistive source degeneration; (c) active degeneration; (d) inductive degeneration

The linearity of differential input differential output (DIDO) transconductors is measured by magnitude of the third order harmonics if a Taylor expansion is performed

on equation $i_{out} = f(v_{in})$ at around DC operation points, where $v_{in} = V_{in+} - V_{in-}$, and $i_{out} = I_{out+} - I_{out-}$.

Since even order harmonics are cancelled due to the differential structure, we can write the equation $i_{out} = f(v_{in})$ as follows after a Taylor expansion at DC operation points($v_{in} = 0$):

$$i_{out} = G_m v_{in} + a_3 v_{in}^3 + a_5 v_{in}^5 + ... \tag{2.24}$$

Source degeneration technique has been widely adopted to increase linear operation range of CMOS circuits. According to the form of degeneration, circuits built using source degeneration techniques fall into three categories: resistive degeneration, active degeneration, and inductive degeneration.

For a simple differential pair transconductor (Figure2.13a), equation of output current in terms of input voltage can be expressed as:

$$i_{out} = \begin{cases} \frac{1}{2} v_{in} \sqrt{bI_{SS}} \sqrt{1 - \frac{b v_{in}^2}{4 I_{SS}}}, when |v_{in}| \le \sqrt{\frac{2I_{SS}}{b}} \\ \frac{1}{2} I_{SS} \operatorname{sgn}(v_{in}), when |v_{in}| \ge \sqrt{\frac{2I_{SS}}{b}} \end{cases} \tag{2.25}$$

$$G_m = \left. \frac{\partial i_{out}}{\partial v_{in}} \right|_{v_{in}=0} = \frac{1}{2} \sqrt{bI_{SS}} \equiv G_{m0}$$

$$a_3 = \left. \frac{\partial^3 i_{out}}{\partial v_{in}^3} \right|_{v_{in}=0} = -\frac{3}{I_{SS}^2} \equiv a_{3,0}$$

……

Performing the same analysis on a resistive source-degenerated transconductor (figure2.13b), we obtain:

$$i_{out}=\begin{cases}\dfrac{1}{2}(v_{in}-i_{out}R)\sqrt{bI_{SS}}\sqrt{1-\dfrac{b(v_{in}-i_{out}R)^2}{4I_{SS}}}, when\left|v_{in}-\dfrac{I_{SS}R}{2}\right|\le\sqrt{\dfrac{2I_{SS}}{b}}\\ \dfrac{1}{2}I_{SS}\,\mathrm{sgn}(v_{in}), when\left|v_{in}-\dfrac{I_{SS}R}{2}\right|\ge\sqrt{\dfrac{2I_{SS}}{b}}\end{cases} \tag{2.26}$$

$$G_m=\left.\frac{\partial i_{out}}{\partial v_{in}}\right|_{v_{in}=0}=\frac{\frac{1}{2}\sqrt{bI_{SS}}}{1+\frac{1}{2}\sqrt{bI_{SS}}\cdot R}=\frac{G_{m0}}{1+G_{m0}R} \tag{2.27}$$

$$a_3=\left.\frac{\partial^3 i_{out}}{\partial v_{in}^3}\right|_{v_{in}=0}=-\frac{3}{I_{SS}^2}\left(\frac{G_{m0}}{1+G_{m0}R}\right)^3=\left(\frac{G_{m0}}{1+G_{m0}R}\right)^3\cdot a_{3,0}=a_{3,1}$$

……

Since $\frac{G_{m0}}{1+G_{m0}R}<1$, we conclude that

$$a_{3,1}<a_{3,0} \tag{2.28}$$

which indicates that transconductors designed using resistive source degeneration approach have better linearity than simple differential pairs.

Shown in figure 2.13(c) is a transconductor with active source degenerations. A pair of MOS resistors M3 and M4 replaces the degeneration resistor, R in figure2.13b. Benefits of active degeneration approach include elimination of extra manufacture steps (to build resistor) and easy control of resistance value. A practical OTA using active degeneration is shown in Figure 2.14. [13]

In RF applications where the requirement on noise performance is very strict, inductive degeneration is used to perform both linearization and input impedance matching (Figure 2.13d). Noise performance of this approach is improved due to the fact

that degeneration inductors are noiseless. However, applications of inductive degeneration are limited at UHF when sizes of on-chip inductors are practical.

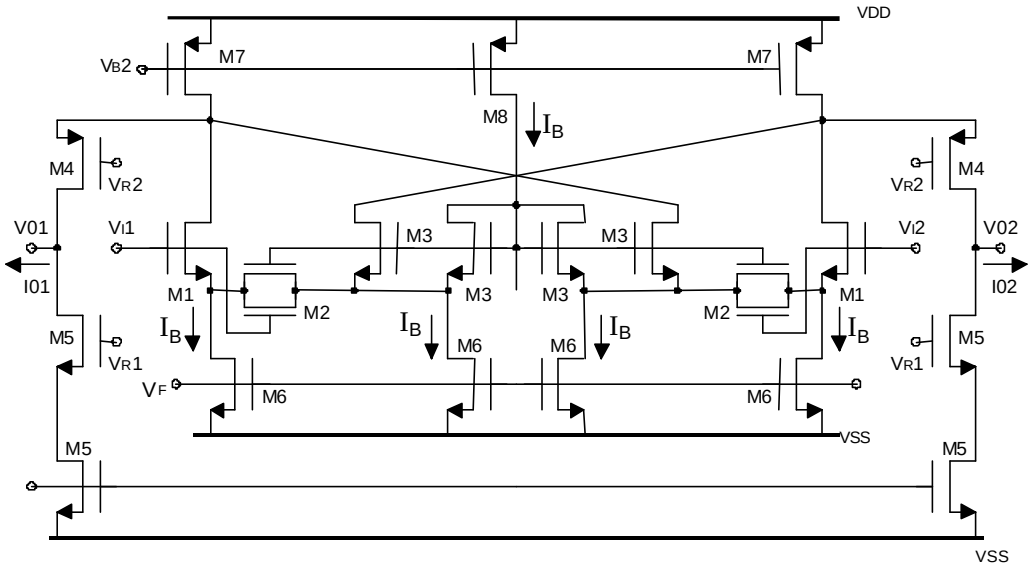


Figure 2.14 A linear transconductor [13]

Advantages of source degeneration approach include: simple circuitry, low power consumption, and suitable for low voltage applications. However, when better linearity is desired and power consumption is not a concern, more complex circuitry such as active biasing approach would be used (figure 2.15) [62-64].

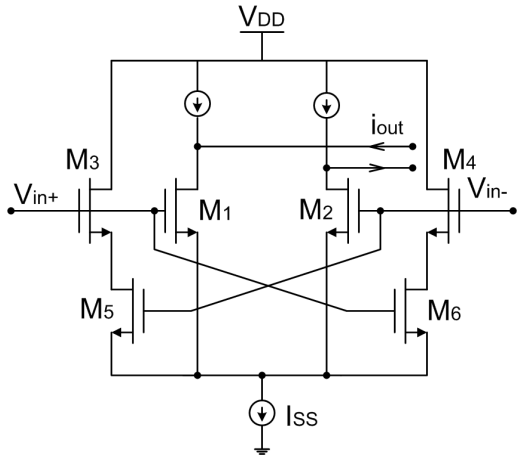


Figure 2.15 A transconductor using active biasing [63]

The idea of improving linearity using active biasing approach originates from the fact that distortion happens when input signal level is large and bias current is not large enough to afford the large amount of transient signal currents induced by the large input voltage. By dynamically increasing bias current when input signal level increases, better linearity is achieved.

Two signal paths are formed in an active biased transconductor circuit. The first signal path, which consists of M_1 and M_2, is the same as a simple differential pair. The second signal path is formed by M_3, M_5, M_4, and M_6. The total bias current I_{SS} is split between the two signal paths. When the ratio of $(W/L)_{1,2}$ to $(W/L)_{3,4}$ is designed to be a certain value [63], M_5 and M_6 dynamically control the amount of bias current flowing through the M_3 and M_4 signal path according to the input signal level since gates of M_5 and M_6 are tied to the input terminals.

Implementation of active biasing circuits requires careful arrangement in layout such that the ratio of $(W/L)_{1,2}$ to $(W/L)_{3,4}$ is precisely controlled. Moreover, compared to

simple linearization approaches such as source degeneration, noise performance is not as good due to the existence of M_3~M_6.

2.5 Q-enhanced LC Filters

As progresses in CMOS technologies enable the designs of high performance integrated passive components, design of integrated filters for gigahertz RF applications becomes possible. To date, progress has been made in the design of Q-enhanced LC filters [45-49].

Q-enhanced LC filters are built based on Q-enhanced LC tanks (Figure2.16). The basic idea is to use a lossy LC tank and boost up Q of filter by incorporating a negative resistance for partial compensation of the loss in the tank. The concept is shown in Figure2.16. Loss in LC tank (Figure2.16a) is mainly caused by the loss of inductor. Assuming the series resistance associated with the inductor, L, is Rs, we define the starting quality factor of the inductor as:

$$Q_0 = \frac{w_0 L}{R_S} \tag{2.29}$$

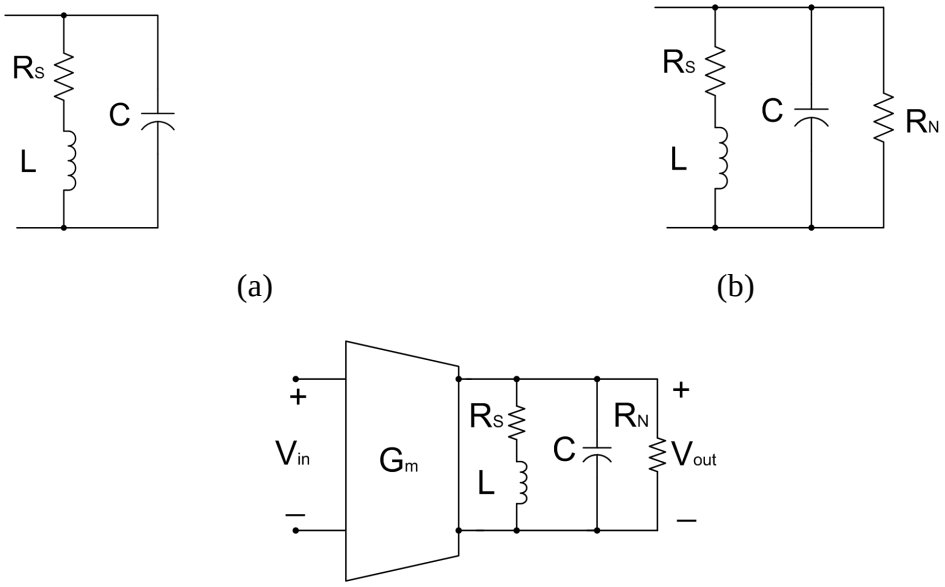


Figure 2.16 (a) A lossy LC tank (b) A Q-enhanced LC tank
(c) A Q-enhanced LC filter

A second-order Q-enhanced LC bandpass filter is shown in Figure2.16(c). The transfer function can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s\frac{1}{C} + \frac{R_S}{LC}}{s^2 + s(\frac{1}{R_N C} + \frac{R_S}{L}) + \frac{1}{LC}(1 + \frac{R_S}{R_N})} \tag{2.30}$$

$$\text{Center frequency} \quad f_0 = \frac{1}{\sqrt{LC}}\sqrt{(1 + \frac{R_S}{R_N})}$$

$$Q = \frac{1}{\sqrt{\frac{L}{C}} \cdot \frac{1}{R_n} + \sqrt{\frac{C}{L}} \cdot R_S} \tag{2.31}$$

The first term in the denominator of (2.31) is negative, which makes the sum of the two terms in the denominator less than the value of the second term, and the Q value is boosted up. To build high Q filters, value of negative resistance, R_N, is designed to be

$$|R_N| > \frac{L}{R_S C} \tag{2.32}$$

Note that R_N must be very close to but larger than $\frac{L}{R_S C}$ to ensure the stability of the filter while achieving high Q. Issues on 1-dB compression dynamic range of Q-enhanced LC filters are discussed in [45]. The 1-dB compression dynamic range can roughly be expressed as:

$$DR = \frac{P_{1-dB}}{4kT(g'+1)BQ^2} Q_0^2 \tag{2.33}$$

where $P_{1\text{-dB}}$ is the 1-dB compression point, g' is a noise parameter and the value is in the order of 1 to 2, B is the 3-dB bandwidth, kT is the product of Boltzmann constant and temperature in Kelvin.

In the calculation of the 1-dB compression point, the input transconductance stage and varactors are assumed to be linear, leaving the negative resistance as the only source of non-linearity. It is clearly seen from (2.33) that the dynamic range of Q-enhanced LC filters strongly depends on Q_0, the starting quality factor of integrated inductors. The reason for this is twofold: first, the higher the Q_0, the smaller the series resistance R_S, and the lower the noise it generates; Second, as R_S becomes smaller, less compensation is desired from the negative resistance, thus smaller DC current is required, resulting in smaller noise currents. Considering nonlinearity effect of input transconductance stage

and varactors, more detailed analysis of dynamic range performance in Q-enhanced LC filters is given in [45].

Design of on-chip inductors plays a dominant role in the design of Q-enhanced LC filters. Numerous research efforts have been devoted to modeling, design and optimization of integrated inductors in CMOS processes. Planar spiral inductors (Figure2.17) have proven to be the most practical ways of implementing inductors on silicon substrate.

Top metal layers are usually used in the design of planar spiral inductors due to greater thickness and larger distance from substrate. It is critical to maximize the quality factor under the constraint of area and process parameters. Factors that affect the Q value of an inductor include: shape (square, hexagonal, octagonal, circular…); geometric parameters (dout, din); number of turns (n); wire width (w) and wire spacing (S). Meanwhile, loss through conductive substrate also decreases the quality factor, as illustrated by a vertical view of a planar spiral inductor on silicon substrate (figure2.18). Accurate modeling of planar spiral inductors has been discussed in literature [59]. Precise and simple models help reduce turnaround time and design cost, and enables faster time to market. A distributed segment-by-segment based inductor model (Figure2.19) exhibits excellent accuracy. However, it complicates circuit simulation by introducing a larger number of model parameters. A lumped model (figure2.20) is widely accepted by designers, modifications have been made to improve the accuracy while keeping the simplicity. To reduce time consumption in simulation, most of the models discussed in literatures are for narrow band applications, ignoring the frequency dependence of series resistance, Rs. Wideband modeling issues are addressed in [60].

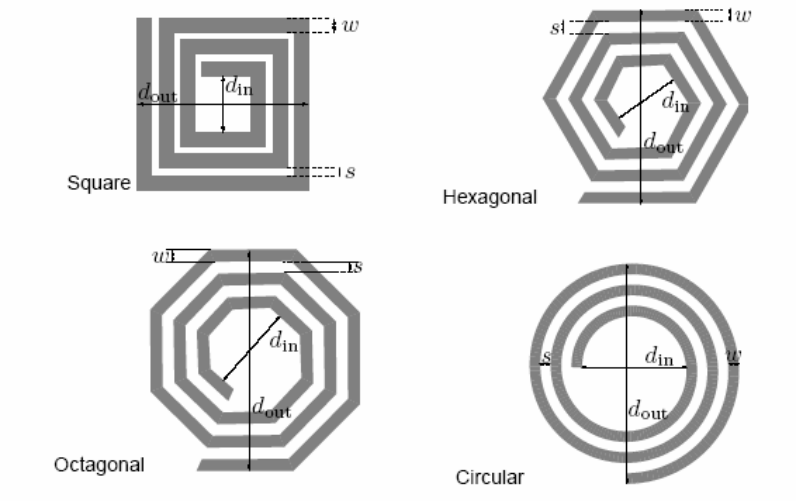


Figure 2.17 Top views of planar spiral inductors

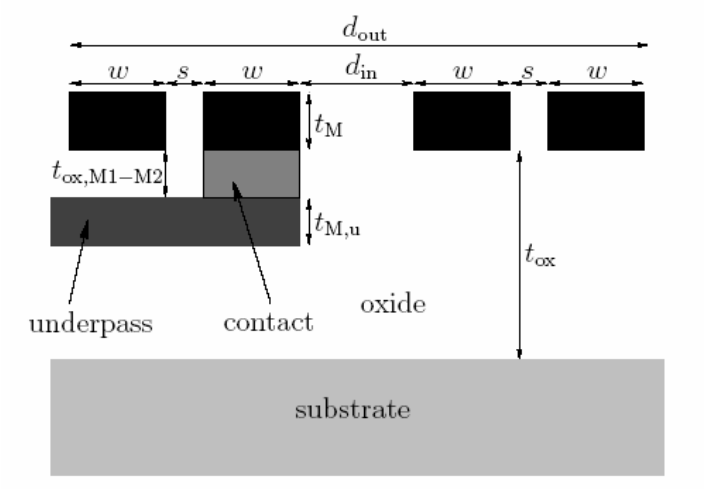


Figure 2.18 Side view of an on-chip inductor

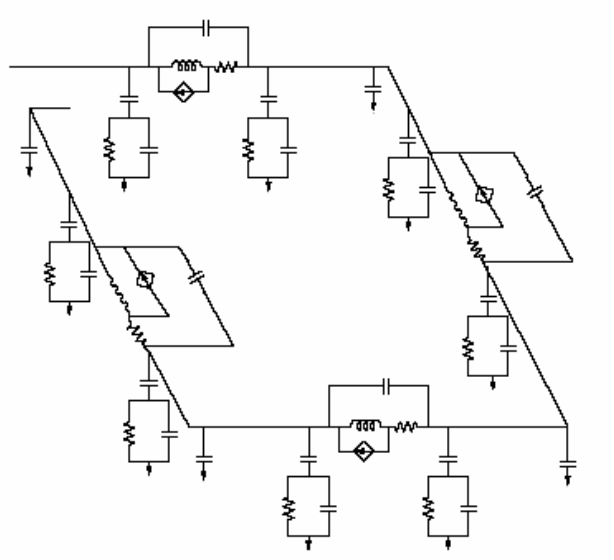


Figure 2.19 A distributed model of on-chip inductor

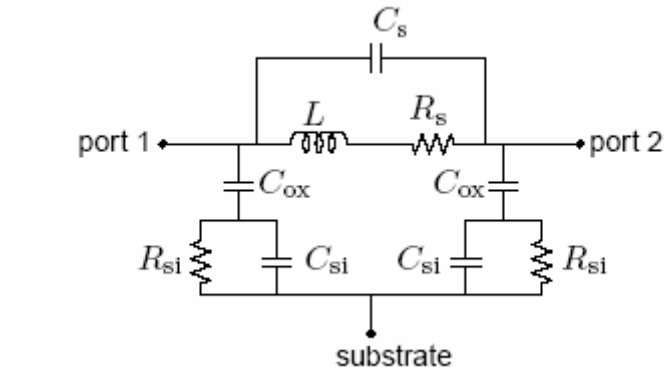
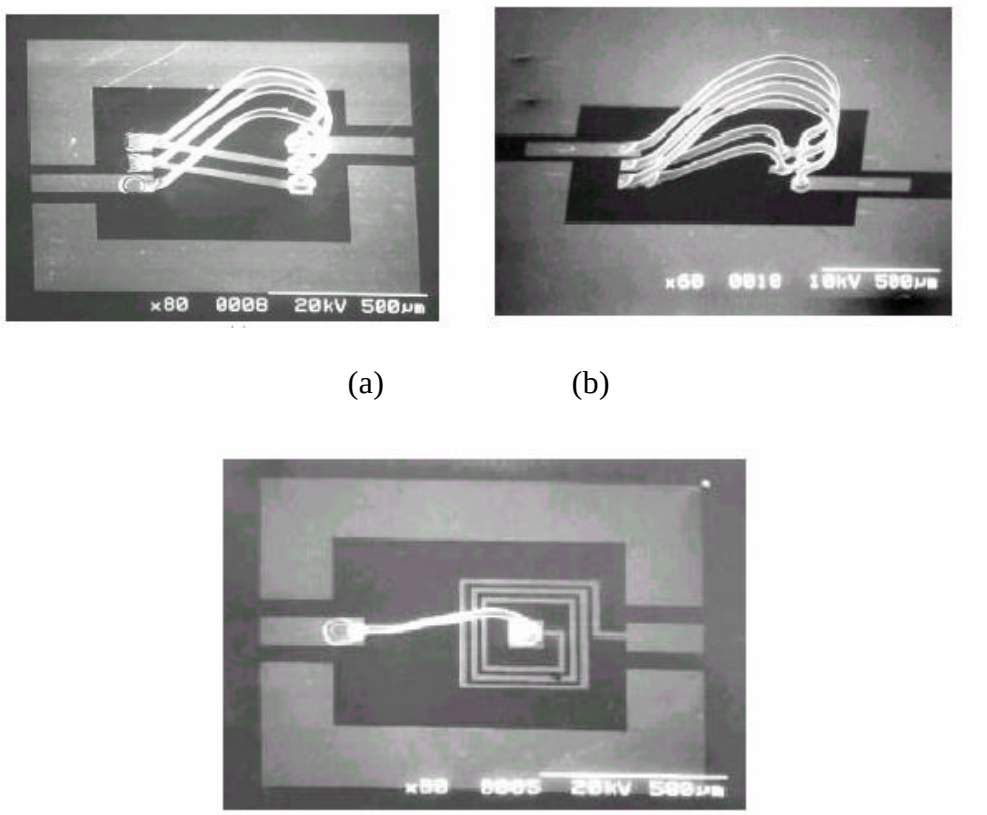


Figure 2.20 A lumped, scaled model on on-chip inductors

Modification of fabrication processes can greatly improve quality factor of an integrated inductor. For example, high-Q inductors can be achieved using wire bonding technologies (figure2.21). Compared to planar inductors, bondwire inductors generally have higher Q due to the fact that it successfully avoid the ohmic loss through metal sheet resistance, and reduces substrate loss by vertical placement of bondwire loops [61].

Several novel on-chip inductors are designed using suspended and multi-layer structures [61].



(a) (b)

(c)

Figure 2.21 Bondwire inductors (a), (b) vertical bondwire inductors (c) a planar spiral inductor with bondwire air-bridge [61]

Although high Q inductors are obtained, alterations to mature standard CMOS processes are not favorable. Complicating the fabrication process not only increases production cost, but also decreases the reliability for mass production.

As many other filters, tuning Q-enhanced LC filters includes tuning of center frequency and quality factor. Q-tuning is achieved by adjusting DC bias current of the

negative resistance circuitry, and center frequency tuning is usually implemented using CMOS varactors. CMOS integrated varactors are studied in [62].

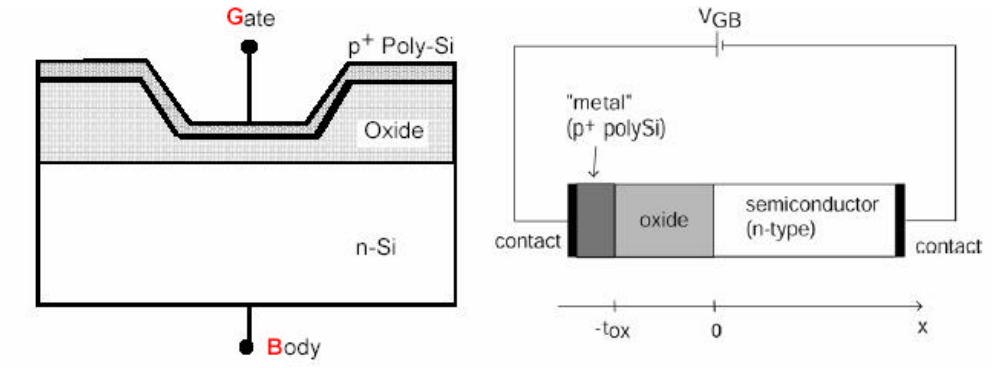


Figure 2.22 Structure of a MOS varactor in n-type silicon substrate. The substrate is grounded and voltage is applied to poly gate

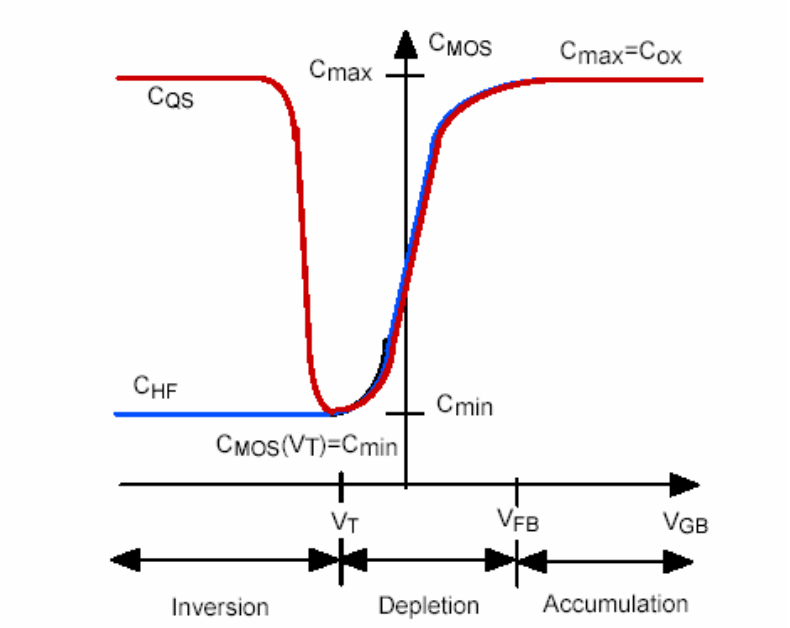


Figure 2.23 Capacitance vs. gate voltage

An example of MOS varactor is shown in figure 2.22. The N-type substrate is connected to ground, and voltage is applied to the poly-silicon gate. As the gate voltage VGB changes, the operation region of MOS varactor changes among inversion, depletion, and accumulation regions. The flatband voltage (V_{FB}) separates the accumulation region from the depletion region, and the threshold voltage (V_{TH}) separates the depletion region from inversion region.

Note that when the varactor operates in inversion region, the capacitance takes two values: C_{HF} and C_{QS}. C_{QS} is quasi-static capacitance, also called low-frequency capacitance, and C_{HF} is high frequency capacitance. At low operation frequencies (<1 kHz), the capacitance value is determined by:

$$C_{MOS,inversion,QS} = \frac{e_{OX}}{t_{OX}} = C_{\max} \tag{2.34}$$

At high frequencies (>1KHz), the generation rate of holes and electrons at the interface of silicon and silicon oxide is not fast enough to allow the formation of a hole charge density at Si/SiO2 interface, and thickness of depletion layer is still at its maximum, resulting in the capacitance to be the minimum value:

$$C_{MOS,inversion,HF} = C_{\min} = C_{depletion,\min} = \frac{C_{ox}C_{D\min}}{C_{ox} + C_{D\min}} \tag{2.35}$$

An important issue in the design of varactors is linearity. To optimize the linearity, capacitance load of a LC tank is divided into two parts: a fixed capacitor and a varactor. Fixed capacitors are usually implemented using more linear poly-poly capacitors. Values of fixed capacitance load are maximized, leaving the varactor just large enough to tune the center frequency.

Another scheme to improve linearity involves discrete tuning. Note that when operating at high frequencies, capacitance values of a CMOS varactor in inversion/accumulation regions are nearly constant as voltage changes, so the capacitance value depends only on the region in which the varactor is working at. If a number of binary weighted array of varactors are connected in parallel, we obtain a discrete tunable varactor with excellent linearity. Fine tuning can be implemented by adding a small varactor working in depletion region. (Figure2.24).The effects of the series resistance caused by switches in Figure 2.24 include: reduced Q of an LC tank and more power in the compensation negative resistance circuit. Meanwhile, since the resistances associated with switches are nonlinear, part of the benefit of this approach is offset and the linearity performance is worse than predicted based on ideal switches.

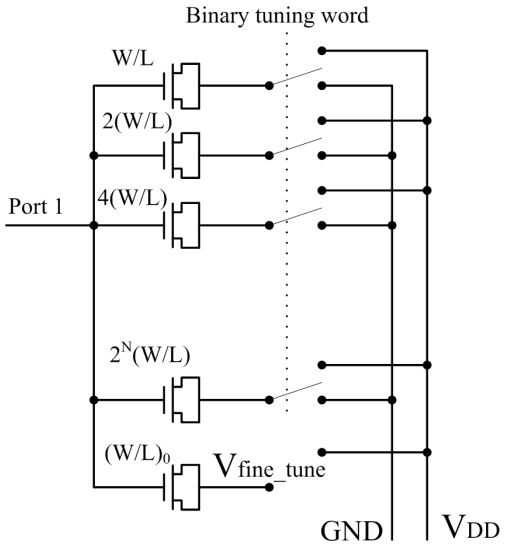


Figure2.24 A linear varactor

2.6 Summary

In this chapter, basic issues in the design of high performance integrated filters are reviewed. Advantages and disadvantages of passive filters, active-RC filters, MOSFET-C

filters, Gm-C filters and Q-enhanced LC filters are studied. A summary is given in Table 2.1

Table 2.1 Summary of high frequency and high Q integrated filters

Filter type	Maximum operation Frequency	Advantages	Disadvantages
Passive	~ 1GHz	Linearity, power, DR	Loss, Q, Size, tunability
Active-RC	~100KHz	Functionality	OPAMPs, tunability
MOSFET-C	~100KHz	Integration	OPAMPs tunability
Gm-C	~1GHz	Tunability, power linearity	Noise
Q-enhanced LC	~10GHz	RF performance Noise	On-chip inductors

We can see that Gm-C filters are most suitable for high frequency applications up to hundreds of megahertz. As to be discussed later, the first system built in this work is a 100MHz low noise and high Q system, implemented using Gm-C techniques.

The only type of filter that would operate properly at several gigahertzes is Q-enhanced LC filters, which makes these filters the only choice for integration of gigahertz RF filters. The second system built in this work is a 2.4GHz low noise and high Q bandpass filter/amplifier, and is categorized as a Q-enhanced LC filter.

CHAPTER 3

SYSTEM ARCHITECTURE

The filter topology investigated in this work originates from an active-RC filter developed by Sallen and Key in 1950s [41]. As shown in Figure 3.1, the Sallen-Key filter is a second-order bandpass filter implemented using two amplifiers and four passive elements. Note that the passive elements R_1, R_2, C_1 and C_2 form a low-Q and lossy second-order bandpass filter, which is referred to as 'the internal passive network' in this work. The Sallen-Key filter itself is referred to as 'the overall filter'.

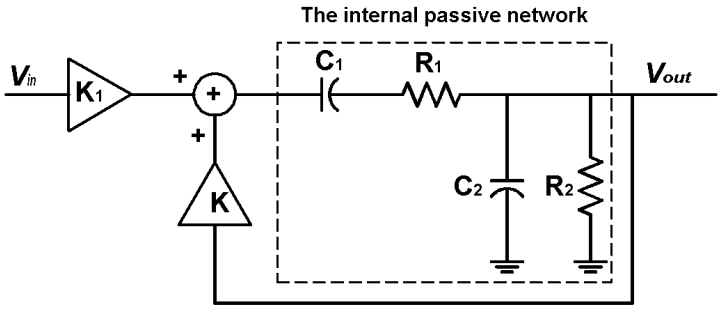


Figure 3.1 A Sallen-Key filter [41]

The transfer function of the filter shown in Figure 3.1 is:

$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{K_1\cdot\frac{1}{C_2R_1}\cdot s}{s^2+s(\frac{1}{C_2R_2}+\frac{1}{C_2R_1}+\frac{1}{C_1R_1}-K\cdot\frac{1}{C_2R_1})+\frac{1}{R_1R_2C_1C_2}}$$

Note that the resonant frequency of the overall filter is the same as that of the internal passive network, and Q factor of the overall filter is determined by Q of the internal passive network and gain of the positive feedback. High-Q values are achieved by careful setting of K. It can be easily proved that positive feedback can be used to build high-Q filters based on the topology shown in Figure3.1, even when other internal passive networks are used.

3.1 System Architecture

The two circuits developed in this work share the same topology architecture, which is shown in Figure 3.2.

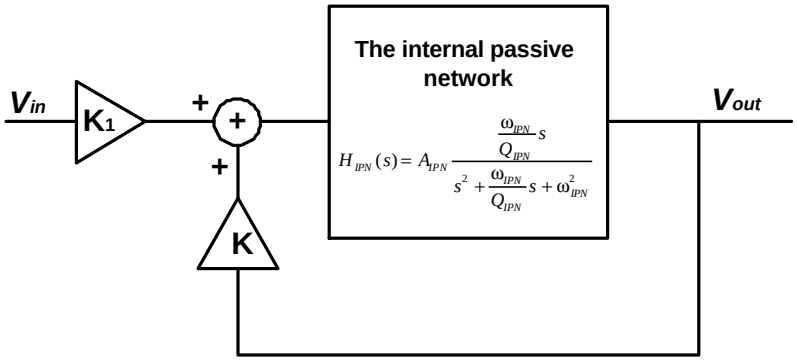


Figure 3.2 System architecture

As shown in Figure 3.2, an internal passive network is built to realize a bandpass transfer function, $H_{IPN}(s)$. For ease of discussion, first assume K_1 and K are ideal amplifiers, i.e., they have zero gain error and infinite bandwidth. Transfer function of the overall filter is derived in (3.1).

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{K_1 \cdot H_{IPN}(s)}{1 - K \cdot H_{IPN}(s)} \tag{3.1}$$

$H_{IPN}(s)$ can be expressed as:

$$H_{IPN}(s) = A_{IPN} \frac{s \cdot \frac{w_{IPN}}{Q_{IPN}}}{s^2 + s\frac{w_{IPN}}{Q_{IPN}} + w_{IPN}^2} \tag{3.2}$$

Rewrite (3.1), we get:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{K_1 \cdot H_{IPN}(s)}{1 - K \cdot H_{IPN}(s)} = \frac{s \cdot K_1 \cdot A_{IPN} \cdot \frac{w_{IPN}}{Q_{IPN}}}{s^2 + s \cdot (1 - K \cdot A_{IPN}) \cdot \frac{w_{IPN}}{Q_{IPN}} + w_{IPN}^2} \tag{3.3}$$

$$H(s) = A \frac{s \cdot \frac{w_0}{Q}}{s^2 + s\frac{w_0}{Q} + w_0^2} \tag{3.4}$$

Comparing with the standard form second-order bandpass transfer function in (3.4), the characteristic parameters such as: center frequency, w_0, Q factor, and pass-band gain of the overall filter can be extracted, as expressed in equation (3.5).

$$\begin{aligned} w_0 &= w_{IPN}, \\ Q &= \frac{Q_{IPN}}{1 - K \cdot A_{IPN}}, \\ A &= \frac{K_1 \cdot A_{IPN}}{1 - K \cdot A_{IPN}}. \end{aligned} \tag{3.5}$$

We can see that the center frequency of the overall filter is the same as that of the internal passive network, which implies that frequency tuning of the overall filter can be achieved by tuning the internal passive network.

Also we can see from (3.4) that the Q value of the overall system is controlled by $K \cdot K_{IPN}$, the product of gain in the feedback path, and midband gain of the internal

passive network. As $K \cdot K_{IPN}$ approaches 1, the Q value can be significantly enhanced, and very high Q values are achieved. A resonator is realized when $K \cdot K_{IPN} = 1$. To ensure stability of the overall system, gain of the feedback path must be accurately controlled, such that the value of $K \cdot K_{IPN}$ is close to but less than 1.

Gain of the overall system is determined by several factors. The most dominant is the input amplifier $K_{1,}$ which determines noise performance. Gain of the overall system also depends on midband gain of the internal passive network, and Q of the overall system.

3.2 Sensitivity Analysis

There are three building blocks in the RF low-noise and high-Q filter system investigated in this work (Figure 3.2): An input amplifier with a gain of K_1; A feedback amplifier with a gain of K; and an internal passive network. The purpose of sensitivity analysis is to identify the most sensitive block(s), variations of which have the most influence on system performance such as: Q, gain, and stability.

Sensitivities of Q with respect to properties of each building block are evaluated as follows. Based on (3.5), we have:

$$S_{Q_{IPN}}^{Q} = \frac{Q_{IPN}}{Q} \cdot \frac{\partial Q}{\partial Q_{IPN}} = 1$$

$$S_{A_{IPN}}^{Q} = \frac{A_{IPN}}{Q} \cdot \frac{\partial Q}{\partial A_{IPN}} = \frac{K \cdot A_{IPN}}{1 - K \cdot A_{IPN}} \tag{3.6}$$

$$S_{K}^{Q} = \frac{K}{Q} \cdot \frac{\partial Q}{\partial K} = \frac{K \cdot A_{IPN}}{1 - K \cdot A_{IPN}}$$

To achieve large Q, $1 - K \cdot A_{IPN} << 1$, and $\frac{K \cdot A_{IPN}}{1 - K \cdot A_{IPN}} >> 1$. According to (3.6), variations of A_{IPN} and K have the most significant influence on Q. To avoid large variations in Q values, the feedback amplifier, K, should be tunable, and the gain should be precisely controlled. Issues in the design of precise and tunable amplifiers will be addressed later in this work.

Based on (3.5), sensitivities of midband gain with respect to properties of building blocks are analyzed as follows:

$$S_{A_{IPN}}^{A} = \frac{A_{IPN}}{A} \cdot \frac{\partial A}{\partial A_{IPN}} = 1 + \frac{K}{1 - K \cdot A_{IPN}}$$

$$S_{K_1}^{A} = \frac{K_1}{A} \cdot \frac{\partial A}{\partial K_1} = 1 \tag{3.7}$$

$$S_{K}^{A} = \frac{K}{A} \cdot \frac{\partial A}{\partial K} = \frac{K \cdot A_{IPN}}{1 - K \cdot A_{IPN}}$$

Again, assume $1 - K \cdot A_{IPN} << 1$, and $A_{IPN} < 1$, we may conclude from (3.7) the following:

$$S_{A_{IPN}}^{A} > S_{K}^{A} > S_{K_1}^{A} \tag{3.8}$$

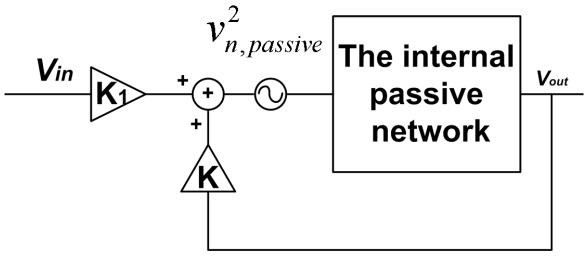
Equation (3.8) implies that the gain of the overall filter is most sensitive to the variations in the gain of the internal passive network.

Note that the term $1 - K \cdot A_{IPN}$ appears in the denominators of several equations in (3.7) and (3.8). To increase $1 - K \cdot A_{IPN}$ helps to improve both Q and gain sensitivities. However, the same term also plays an important role in deciding values of Q and gain. Large value of Q_{IPN} helps to keep Q as large as desired while having a large value of $1 - K \cdot A_{IPN}$, which helps improve overall sensitivity performance. This coincides with the

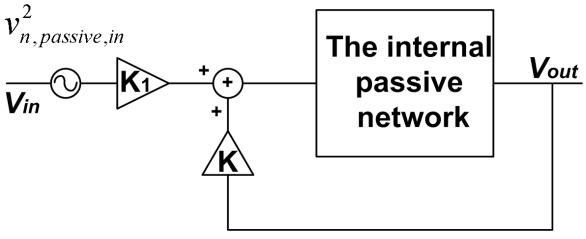
common statement that having large Q values in the internal passive network enhances system performance.

3.3 Noise Analysis

As stated earlier, the circuits built in this work consist of three parts: the input stage, the internal passive network, and the positive feedback amplifier. To perform noise analysis, assuming that the noise generated by each of the three building blocks is purely random, and are independent of each other. The analysis is performed by first extracting the equivalent input noise of each part while assuming the other two parts are noiseless, and then sum up the equivalent input noise of all three parts.



(a) Noise from the internal passive network

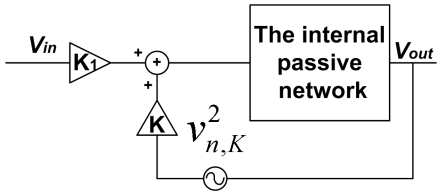


(b) Equivalent input noise

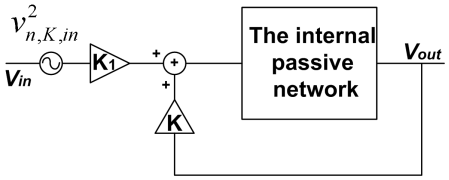
Figure 3.3 Noise analysis – the internal passive network

As illustrated by Figure 3.3, let $v^2_{n,passive}$ denote the input referred noise of the internal passive network. The equivalent noise referred to the system input terminal is $v^2_{n,passive,in}$.

$$v^2_{n,passive,in} = \frac{(1 - K \cdot H_{IPN}(jw))^2}{K_1^2} v^2_{n,passive} \tag{3.9}$$



(a)



(b)

Figure3.4 Noise analysis – the feedback amplifier

(a) Noise generated from the feedback amplifier (b) Equivalent input noise

As illustrated by Figure 3.4, let $v^2_{n,K}$ denote the input referred noise of the amplifier in the positive feedback path, and $v^2_{n,K,in}$ is the equivalent noise power at the system input.

$$v^2_{n,K,in} = \frac{(1 - K \cdot H_{IPN}(jw))^2}{K_1^2 H_{IPN}(jw)^2} v^2_{n,K} \tag{3.10}$$

Shown in Figure 3.5 is the input equivalent noise of the input amplifier, K_1.

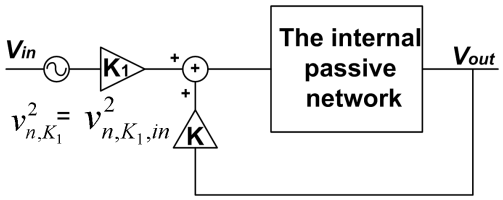


Figure 3.5 Noise analysis – the input stage

Since noise generated from each individual stage is independent, the overall noise power is the sum of noise from each individual stage.

$$\begin{aligned} v_{n,input,in}^2 &= v_{n,passive,in}^2 + v_{n,K,in}^2 + v_{n,K_1,in}^2 \\ &= \frac{(1-K\cdot H_{IPN}(jw))^2}{K_1^2 H_{IPN}(jw)^2} v_{n,K}^2 + \frac{(1-K\cdot H_{IPN}(jw))^2}{K_1^2} v_{n,passive}^2 + v_{n,K_1,in}^2 \end{aligned} \tag{3.11}$$

To find out the significance of noise from each individual stage, the magnitudes of coefficients in each term of (3.11) are evaluated at the center frequency. In general, gain of the internal passive network is less than 1 due to the loss of passive elements, so we can conclude that:

$$\left|\frac{(1-K\cdot H_{IPN}(jw))^2}{K_1^2 H_{IPN}(jw)^2}\right| > \left|\frac{(1-K\cdot H_{IPN}(jw))^2}{K_1^2}\right| \tag{3.12}$$

Furthermore, the gain of high Q filters at resonant frequency is generally proportional to Q, thus is a relatively large value. Note that the coefficient of $v_{n,K,in}^2$ is a reciprocal of the system transfer function shown in equation (3.11).

$$\begin{aligned} Q >> 1 &\Rightarrow \left|\frac{K_1^2 H_{IPN}(jw)^2}{(1-K\cdot H_{IPN}(jw))^2}\right|_{w=w_0} \propto Q >> 1 \\ &\Rightarrow \left|\frac{(1-K\cdot H_{IPN}(jw))^2}{K_1^2 H_{IPN}(jw)^2}\right|_{w=w_0} << 1 \end{aligned} \tag{3.13}$$

Combining (3.12) and (3.13), we can see that the noise generated by the input amplifier K_1 has the most significant influence on system noise performance. It is critical to have enough gain in the input stage to improve the overall noise performance. It is seen that the effect of the noise generated from the feedback amplifier is more significant than that of the internal passive network.

3.4 Linearity Analysis

To identify the bottleneck of linearity performance, maximum ac signal levels are evaluated at each node of the system. Linearity analysis is carried out by observing the maximum signal level at the input of each individual stage to identify the bottleneck.

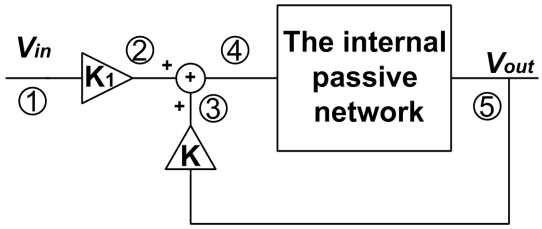


Figure 3.6 System diagram with node labels

Table 3.1 maximum AC signal levels

Node	Maximum signal level (volt)
①	$V_{in,\max}$
②	$K_1 \cdot V_{in,\max}$
③	$\frac{K \cdot K_1 \cdot A_{IPN}}{1 - K \cdot A_{IPN}} V_{in,\max}$
④	$\frac{K_1}{1 - K \cdot A_{IPN}} V_{in,\max}$
⑤	$\frac{K_1 \cdot A_{IPN}}{1 - K \cdot A_{IPN}} V_{in,\max}$

To find out which node has the largest AC signal level, we need to compare terms in the second column of Table3.1. Note that node ① is input node, and node ⑤ is output node. Recall from equation (3.5), to achieve high Q, we need:

$$1 - K \cdot A_{IPN} << 1$$

$$\Rightarrow \quad \frac{K_1}{1 - K \cdot A_{IPN}} V_{in,\max} > K_1 \cdot V_{in,\max} \tag{3.14}$$

=> maximum signal level at node ④ > maximum signal level at node ②

On the other hand, to make the system stable, we need:

$$1 - K \cdot A_{IPN} > 0 \Rightarrow K \cdot A_{IPN} < 1$$

$$\Rightarrow \quad \frac{K_1}{1 - K \cdot A_{IPN}} V_{in,\max} > \frac{K \cdot K_1 \cdot A_{IPN}}{1 - K \cdot A_{IPN}} V_{in,\max} \tag{3.15}$$

=> maximum signal level at node ④ > maximum signal level at node ③

As mentioned above, midband gain of the internal passive network is less than one due to the lossy nature of passive elements, which implies:

$$A_{IPN} < 1$$

$$\Rightarrow \frac{K_1}{1 - K \cdot A_{IPN}} V_{in,\max} > \frac{K_1 \cdot A_{IPN}}{1 - K \cdot A_{IPN}} V_{in,\max} \tag{3.16}$$

=> maximum signal level at node ④ > maximum signal level at node ⑤

From equations (3.14) ~ (3.16), it is clearly seen that the largest ac signal level appears at node ④. This implies that the internal passive network, which stays right next to node ④ in the signal path, must have superior linearity performance to reduce distortions due to large input signals. To achieve this, integrated passive components with better linearity are preferred. For example, poly-poly capacitors help to improve the overall linearity of the system much better than MOS capacitors; also, poly resistors bring much better linearity than MOS diode resistors.

However, for some applications it is necessary to implement passive components by active means. For example, MOS varactors must be used instead of poly-poly capacitors to tune resonant frequencies; diode resistors must be used considering matching issues, etc. When CMOS based passive elements are designed, linearity issues can be taken care of by one of more approaches, such as: increase DC bias current; increase gate overdrive voltages of critical transistors; or carefully bias the critical transistors in the most linear operation region (usually in triode region), etc.

The next important part concerning the linearity issue is the amplifier in the positive feedback path. Signal level at the input of this amplifier is the second largest in Table 3.1 This is more obvious when the system is implemented using current-mode approach. The amplifier becomes current amplifiers/mirrors in current mode implementations. Current signals at output of current amplifiers are inherently large,

causing distortions if dc bias current source is not enough to provide the large amount of varying current.

3.5 Implementation Using Current-mode Approach

A conventional voltage-mode implementation of the system in Figure 3.2 is given in Figure 3.7. The input and feedback amplifiers are realized by G_{m1} and G_{m2}. A voltage buffer is inserted in front of the internal passive network to drive the large passive load.

3.5.1 Problems with Voltage-mode Implementation

As shown in Figure3.7, the input transconductor and the finite gain amplifier are combined as a dual-input transconductor (G_{m1}). G_{M1} is a dual-input single output transconductor amplifier: one of the two input terminals takes system input voltages, the other takes the feedback signal from the output of the passive network. In G_{m1}, drains of the two differential pairs are coupled together to sum up currents generated from the input and the feedback paths. The sum current is then converted to voltage by a diode connected transconductor G_{m2}.

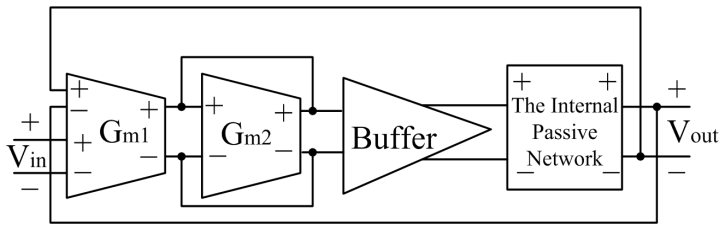
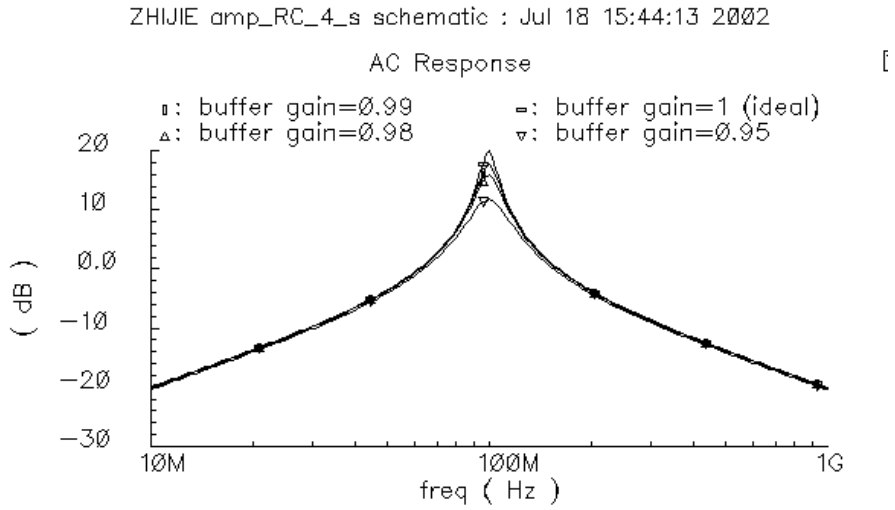


Figure 3.7 an example of voltage-mode implementation

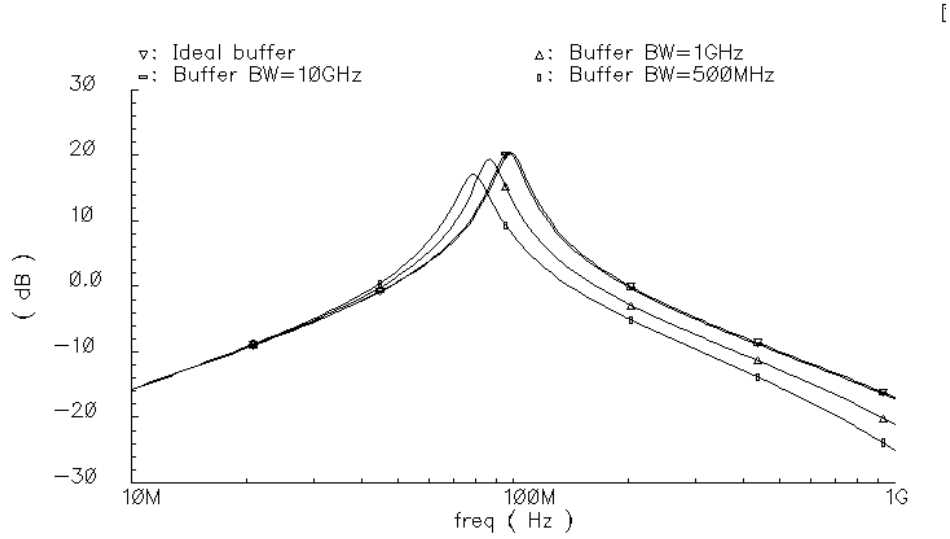
At the output of G_{m2}, a voltage buffer is designed to drive the passive network. Ideally, a voltage buffer has gain of 1 and infinite bandwidth. Difference between gain of the buffer and 1 is defined as the gain error of the buffer. Simulations are performed to reveal effects of gain error and finite bandwidth of the buffer on performance of the system. Assume the resonant frequency of the passive network is 100MHz and Q=10. The macro-model simulation results are shown in Figure 3.8.

As shown in Figure 3.8(a), Q and pass-band gain of the system are very sensitive to gain error of the buffer. When gain of the buffer changes from 1 to 0.99 (1%), gain of the system changes from 19.7dB to 17.45dB (23%), and the Q changes from 9.1 to 7.1 (22%). We conclude that as the gain of the buffer decreases, the filter suffers from the losses of both gain and Q.

Figure 3.8(b) shows the effect of the finite buffer 3-dB bandwidth on system frequency response. As the buffer bandwidth decreases, the center frequency shifts from the desired value, the gain decreases, and Q decreases as well. From Figure 3.8(b), we see that, to maintain the desired frequency transfer function, the buffer bandwidth should be at least 1GHz.



(a)



(b).

Figure 3.8 Effect of buffer nonidealities on filter response

(a) Effect of buffer gain error on AC magnitude response

(b) Effect of buffer gain error and bandwidth on AC magnitude response

To further explain the point that a buffer is not practical in this design, an example of a source follower as a buffer is given below in Figure 3.9.

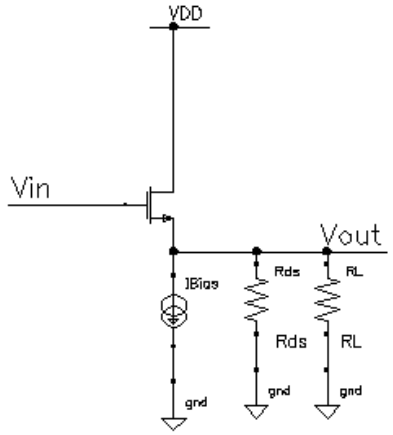


Figure 3.9 A source follower

The gain of the source follower is:

$$A = \frac{g_m (R_L // R_{ds})}{1 + g_m (R_L // R_{ds})} \tag{3.17}$$

To make $A > 0.99$, $g_m (R_L // R_{ds})$ must be greater than 100, R_L should be much less than R_{ds}. Assume R_L is 50Ω. To make $g_m (R_L // R_{ds}) > 100$, g_m should be at least 2000mS. Obviously, it is not practical to build a transconductor whose g_m is 2000mS. Assume a reasonable value for g_m, for example, 20mS. The gain of the buffer is:

$$A = \frac{20mS \cdot 50\Omega}{1 + 20mS \cdot 50\Omega} = 0.5$$

Obviously a buffer with a gain of 0.5 will seriously deteriorate the performance of the filter. To summarize, implementing the systems in this work is not practical in terms of power consumption and sensitivity due to voltage buffers.

3.5.2 Current-mode Implementation

Systems implemented using current-mode approach take current signals as input, use current feedback and current amplifiers to generate poles and zeros instead of voltage feedback and voltage amplifiers as in voltage-mode circuits. Compared to voltage-mode designs, current-mode systems benefit from wide bandwidth, high speed, low voltage and power, large dynamic range, and simple circuitry [54][63].

As mentioned previously, most designs using voltage-mode approach require I→V conversion circuits and voltage buffers. This is due to the fact that an input differential pair always converts input voltage to current while pre-amplifying input voltage signals for further processing, and we must convert the current signals back to voltage signals to interface other voltage-mode building blocks. I→V conversion stages and voltage buffers can be avoided if we choose to use the current-mode approach.

A current-mode system diagram of the proposed filter is shown in Figure 3.10. The overall transfer function can be expressed as:

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{K_1 \cdot H_{IPN\_I}(s)}{1 - K \cdot H_{IPN\_I}(s)} \tag{3.18}$$

where $H_{IPN\_I}(s)$ is the current transfer function of the current-mode RC bandpass network. Assume

$$H_{IPN\_I}(s) = \frac{A_{IPN\_I} \cdot s \cdot \frac{w_{IPN\_I}}{Q_{IPN\_I}}}{s^2 + s \cdot \frac{w_{IPN\_I}}{Q_{IPN\_I}} + w_{IPN\_I}^2} \tag{3.19}$$

where A_{IPN_I} , Q_{IPN_I} , w_{IPN_I} are the gain, Q and resonant frequency of the current-mode RC bandpass network, respectively. The current transfer function of the system can be expressed as:

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{K_1 \cdot A_{IPN\_I} \cdot s \cdot \frac{w_{IPN\_I}}{Q_{IPN\_I}}}{s^2 + (1 - K \cdot A_{IPN\_I}) \cdot s \cdot \frac{w_{IPN\_I}}{Q_{IPN\_I}} + w_{IPN\_I}^2} \tag{3.20}$$

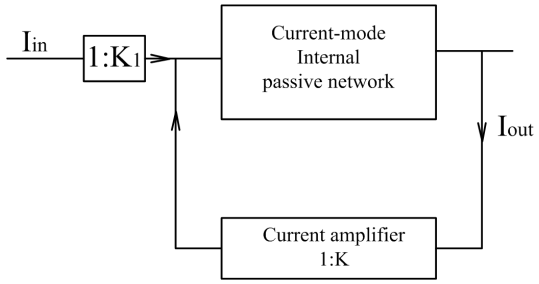


Figure 3.10 Current-mode filter diagram

3.5.3 Current-mode Passive Network

Since it is more convenient to find appropriate topologies of voltage mode networks than current mode networks, it is desirable to obtain the topology of current-mode passive networks from their voltage-mode counterparts and then apply proper system transformations.

The system equation of a two-port system can be expressed as:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

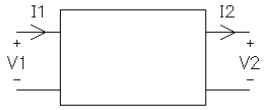


Figure 3.11 A two-port system

Note that:

$$\frac{V_2}{V_1}\Big|_{I_2=0} = \frac{Z_{11}}{Z_{21}}$$

$$\frac{I_1}{I_2}\Big|_{V_1=0} = -\frac{Z_{11}}{Z_{12}}$$

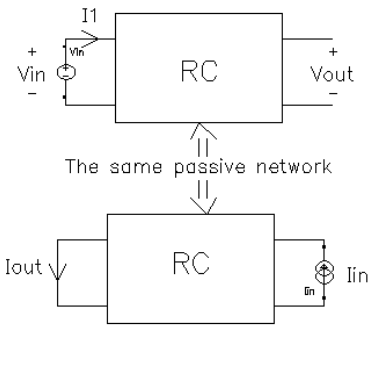
We also know that for a linear passive system, the system characteristic matrix is always symmetric, i.e.

$$Z_{12} = Z_{21}.$$

This leads to the following equation:

$$\frac{V_2}{V_1}\Big|_{I_2=0} = -\frac{I_1}{I_2}\Big|_{V_1=0}$$

We can conclude from above discussion that a current-mode network can be built as the same network that realizes the same form of a voltage transfer function if we replace the input voltage source with a short wire and place an input current source at the output port of the voltage-mode network. The transformation is explained in Figure 3.12.



$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{I_{out}(s)}{I_{in}(s)}$$

Figure 3.12 Transform from voltage mode to current mode

3.5.4 Interface of Current Amplifiers with Passive Network

Current amplifiers are implemented using current mirrors. In general, it's desirable to have the input resistance of a current mirror as small as possible, ideally zero. In this design, the interface between the current amplifier and the internal passive network is simplified. The input resistance of the current amplifier can be designed such that we can remove the resistor that would otherwise be in series with the input of the current amplifier, as illustrated in Figure 3.13.

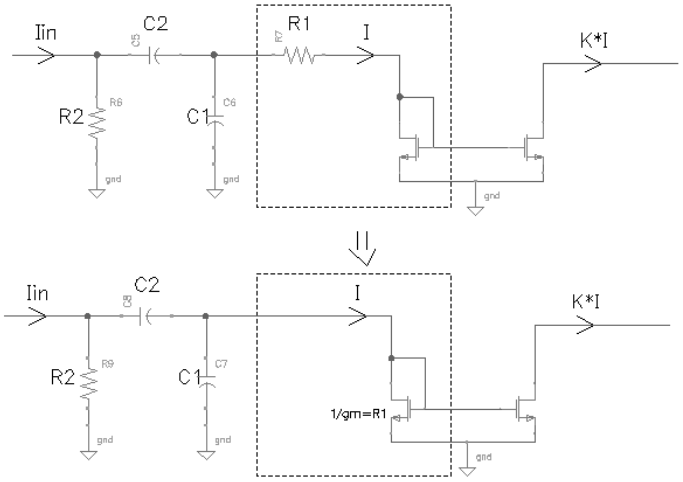
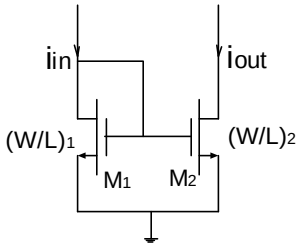


Figure 3.13 Interfacing of passive network with a current amplifier

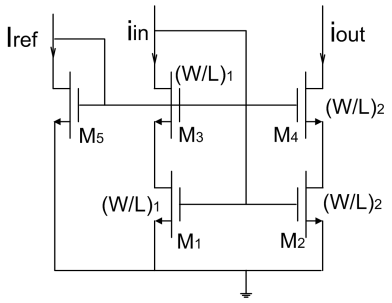
3.5.5 Current Amplifiers

Current amplifiers are implemented using current mirrors. The current gain of a current amplifier is determined by the ratio of W/L's of mirror transistors. When compared to a voltage amplifier, whose gain is determined by the product of transconductance and impedance, the gain of a current amplifier is less sensitive to bias condition. Ideally, a current amplifier has zero input impedance and infinite output impedance, and the gain is accurately defined by the ratio of W/L's. However, the gain of current amplifiers exhibit inaccuracies due to body effects and mismatches in layouts.

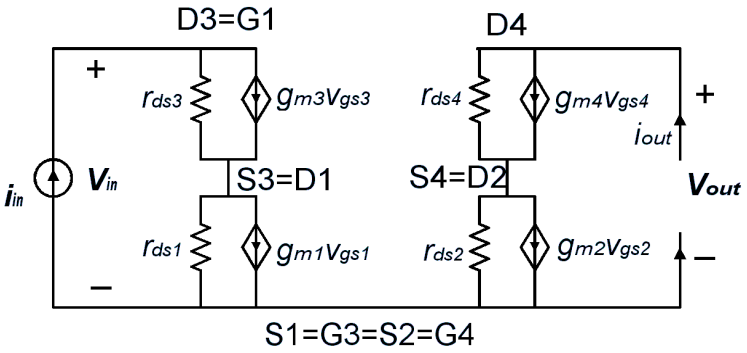
Wide-swing cascode current amplifiers are designed for this work. Compared to simple current amplifiers shown in Figure 3.14(a), a wide-swing cascade (Figure 3.14(b)) achieves better gain accuracy, larger output swing, and larger value of output resistance [52].



(a) a simple current amplifier



(b) a wide swing cascode current amplifier



(c) small signal circuit of (b)

Figure 3.14 a study of current amplifiers

As shown in Figure 3.14(b), the wide-swing current amplifier consists of main current amplification transistors M_1 and M_2, two cascade transistors, M_3 and M_4, and bias transistor M_5 to properly set up the operation points of M_3 and M_4.

It is important to design the input impedance of the wide-swing cascade current amplifier with a small value such that the internal passive network precedes the current amplifiers operates properly. The input impedance of circuit shown in Figure 3.14(b) can be calculated using the small signal equivalent circuit shown in Figure 3.14(c).

$$v_{in} = (i_{in} - g_{m3}v_{gs3})r_{ds3} + (i_{in} - g_{m1}v_{gs1})r_{ds1}$$

$$v_{gs1} = v_{in}$$

$$-v_{gs3} = v_{in} - (i_{in} - g_{m3}v_{gs3})r_{ds3}$$

$$\rightarrow \quad R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1}}{g_{m1}r_{ds1} + g_{m1}g_{m3}r_{ds1}r_{ds3}} \approx \frac{1}{g_{m1}} \tag{3.21}$$

The wide-swing cascode current amplifier has excellent gain accuracy since v_{ds1} and v_{ds2} are always the same. The output impedance of the circuit is:

$$R_{out} \approx g_{m4}r_{ds4}r_{ds2} \tag{3.22}$$

AC response of the wide-swing cascode current amplifier is determined by poles associated with drain of M_1 and M_2, which are connected to the source of M_3 and M_4.

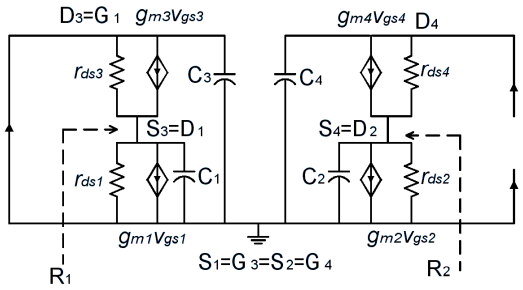


Figure 3.15 small signal equivalent circuit of Figure 3.14(b) with parasitic capacitance

Parasitic capacitances are represented by C1-C4,

$$C_1 = C_{GS3} + C_{BS3} + C_{GD1} + C_{BD1}$$

$$C_2 = C_{GS4} + C_{BS4} + C_{GD2} + C_{BD2}$$

$$C_3 = C_{GS1} + C_{GD3} + C_{BD3}$$

$$C_4 = C_{GS2} + C_{GD4} + C_{BD4}$$

The resistance seen from the drain of M_1 is:

$$R_1 = \frac{1}{g_{m3}}$$

The resistance seen from the drain of M_2 is:

$$R_2 = \frac{1}{g_{m4}}$$

Based on above observation, dominant pole frequencies of the wide-swing cascode current amplifiers can be expressed as follows:

$$p_1 = \frac{1}{R_1 C_1} = \frac{g_{m3}}{C_{GS3} + C_{BS3} + C_{GD1} + C_{BD1}} \tag{3.23}$$

$$p_2 = \frac{1}{R_{12} C_2} = \frac{g_{m4}}{C_{GS4} + C_{BS4} + C_{GD2} + C_{BD2}} \tag{3.24}$$

M_3 and M_4 are designed to have same aspect ratios as M_1 and M_2, respectively. As a result, gm3 is the same as gm1; also gm2 the same as gm4. The transconductances gm1 and gm2 ranges from 10mS to 20 ms to achieve low input impedance of current amplifiers, also to make the passive network that precedes the current amplifier function properly. The transconductances gm3 and gm4 have the same value. Parasitic capacitances are reduced by choosing short channel length (L=0.5um), parasitic poles p1 and p2 having much higher frequencies than the center frequency of the filter.

3.5.6 Variable Gain Current Amplifiers

Shown in Figure 3.14(b) is a fixed gain current amplifier whose gain is predetermined by the ratio of gm2 and gm1. However, as mentioned earlier, Q of the overall filter is controlled by the gain in positive feedback path, which is the gain of the current amplifier. It's desirable to have variable gain in current amplifiers.

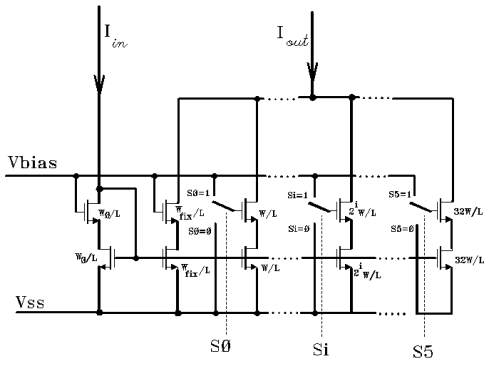


Figure 3.16 a variable gain current amplifier

Shown in Figure 3.16 is a variable gain current amplifier based on the wide swing cascode circuit shown in Figure 3.14 (b). The output current, i_{out}, is the sum of current flowing through the drains of M_{fixed}, M_0, M_1 … and M_5. The current gain $A_I = \frac{i_{out}}{i_{in}}$ is controlled by switches S0-S5. When S_i is open, gate of M_i is connected to VSS, putting Mi in cut-off region, thus current flowing through drain of M_i is zero. When Si is closed, gate of Mi is connected to V_{bias}, enabling current flow through the drain of M_i. Sizes of M_0, M_1…M_5 are binary weighted such that 32 consecutive values of current gain can be achieved at a fixed interval.

In practical designs, as currents are switched in and out of a current amplifier, corresponding bias PMOS transistors should also be switched in and out of the system to maintain stable common mode performance.

In Chapter 3, the system architecture investigated in this work is presented. Block level analyses are performed to identify the design bottlenecks, and provide guidelines in the design of the two circuits to be discussed in Chapter 4 and 5.

CHAPTER 4

A 100MHz LOW-NOISE HIGH-Q FILTER

FOR FM RADIO APPLICATIONS

4.1 A Novel FM Radio Front-end

4.1.1 Integrated FM Radio Receiver

Today's cell phones perform more functions than just making and receiving phone calls. Using cell phones, we can access Internet, browse the web wirelessly and even view webpages in full color. We can access our emails as well as read and send messages. The trend in the development of the cell phone market is to replace all portable devices by one mobile terminal that combines a cell phone, PDA, radio set and wireless office into one device.

Figure 4.1 A Nokia cell phone with an integrated FM radio receiver

Figure 4.1 shows a Nokia 8310 cell phone that features an integrated FM radio receiver as well as instant access to mobile internet services. The unit weighs 3oz, and the size is $97 \times 43 \times 19mm$ [29].

Most FM receivers in today's market use off-chip SAW filters and discrete passive elements to perform impedance matching, filtering and tuning, making the number of off-chip components in a FM receiver to be around fifty. A Philip's FM receiver, TEA5757H, is used in the previously mentioned Nokia 8310 cell phone [31], and there are more than 40 off-chip passive elements, most of which are for filtering and matching purposes. Even though in some FM receivers, such as a Motorola's FM receiver, MC3362, described in [30], the number of discrete components is reduced due to the absence of LNA and image rejection filters, three are still around 25 off-chip passive elements. A large number of off-chip components prohibit the design of compact light-weight portable mobile units. Motivation of this research is to develop a single-chip FM radio receiver that reduces the number of off-chip components.

4.1.2 A Study of Radio Spectrum

A study of the radio spectrum is performed for a better understanding of the filtering/attenuation requirements. As shown in Figure 4.2, the FM radio frequencies lie in the VHF band, together with strong interferers from other signal bands such as cordless phones, televisions, amateur radios, etc. Table 4.1 shows the details of frequency allocation in the VHF band [32].

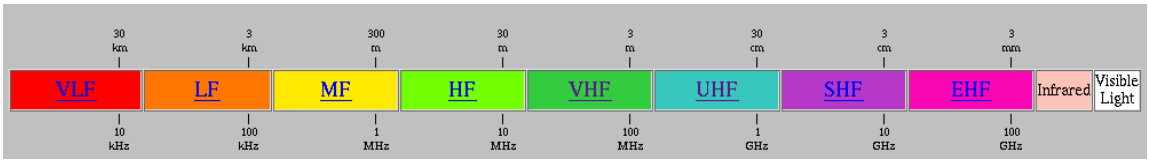


Figure 4.2 Radio Spectrum

Table 4.3 Frequency allocations in the vicinity of 100MHz

Frequencies (MHz)	Descriptions
43~50	Cordless Telephone Base Transmitter
50~54	Amateur
54~72	Broadcast (TV)
72~73	Public Mobile, Private Mobile, Personal Radio
74.8~75.2	Aviation
75.4~88	Public Mobile, Private land mobile, Personal Radio, Broadcast (TV), auxiliary broadcasting
88~108	Broadcast radio(FM), auxiliary broadcasting
117~136	Aviation
136~138	Satellite communications
144~148	Amateur

From Table 4.1 we can see that the FM radio frequency band is close to the broadcast TV (54~88MHz), aviation band (117~136MHz) and satellite band

(136~138MHz). The FM radio band contains 100 broadcasting channels, with each channel occupies 200 KHz bandwidth. The front-end of an FM radio receiver must provide enough selectivity and out of band attenuation to prevent interference from undesired signals.

4.1.3 Architectures Considerations

Filters play important roles in wireless receivers. As we notice from the study of radio spectrum, strong interference exists in frequency bands that are very close to the desired ones. All these interfering signals must be sufficiently attenuated such that they would not saturate receiver front-ends circuits. As a result, in-band-selection/out-of-band rejection filters are required. Image rejection filters are also required in all receivers to suppress image signals. These filters work at very high frequencies and must be low noise.

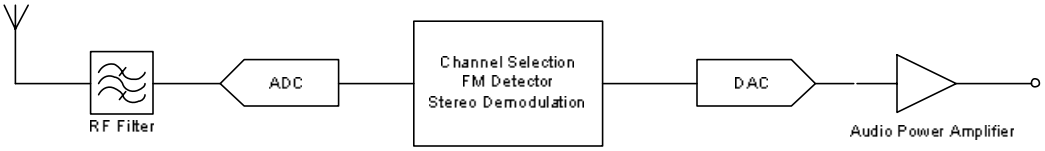
After the received RF signals are down-converted to IF signals, further filtering is performed by either analog channel selection filters or digital filters. For direct down-conversion receivers, channel selection is usually done digitally. In heterodyne receivers, channel selection requires very high-Q and large dynamic range analog filters. A lot of effort has been devoted to the study of both architectures, and the pros and cons of both have been extensively studied [55].

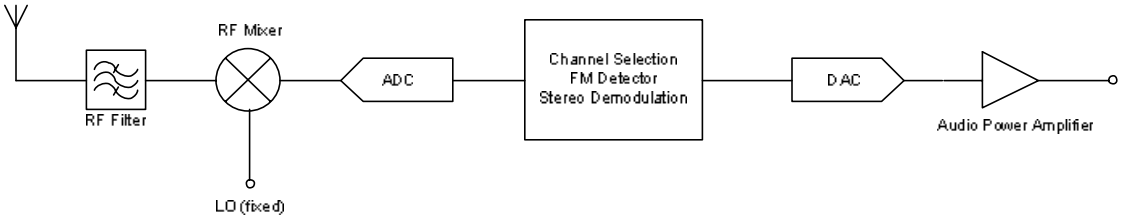
According to the way filtering is achieved, wireless receiver architectures fall into two categories. One type of wireless receivers uses digital filters to perform all channel-selection filtering and thus demand A/D converters operating at very high speed with a large dynamic range. The other type of wireless receivers uses analog filters to

perform complete channel-selection filtering, and relax the requirements on ADCs. In this work, we name the first type of receiver architectures “ADC and digital intensive wireless receivers”, and the second “analog filtering intensive wireless receivers”. A case study of how two categories of architectures can be examined to build a FM radio receiver is conducted in this research.

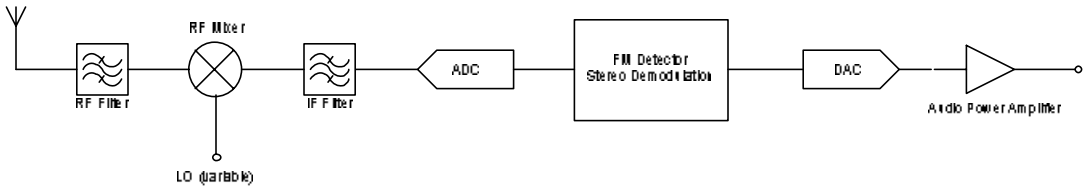
4.1.3.1 ADC and Digital Intensive Wireless Receivers

ADC and digital intensive receivers (Figure 4.3 (a) and (b)) perform all channel-selection filtering digitally. The bandwidth of the RF filter is 20MHz, the same as the signal bandwidth. The ADC operates on the entire 20MHz signal band. In Figure 4.3(a), the ADC works at 100MHz, converts signals in all FM channels into digital signals, and then passes to a digital processor. In Figure 4.3(b), the system architecture is very similar to Figure 4.3(a) except that the ADC works at the IF frequency. The LO frequency is fixed, and all channels are converted into a digital signal.


RF Filter
ADC
Channel Selection
FM Detector
Stereo Demodulation
DAC
Audio Power Amplifier


RF Filter
RF Mixer
LO (fixed)
ADC
Channel Selection
FM Detector
Stereo Demodulation
DAC
Audio Power Amplifier

integrated in CMOS processes are not practical for use as RF filters due to noise and stability concerns [7].



Consider the direct conversion receiver shown in Figure 4.3(b). Instead of selecting the whole FM band, a tunable RF filter selects part of the band which includes the desired channel. The partial RF band is then down-converted into digital signals, and further channel-selection is done digitally.

By distributing the filtering between analog and digital parts of a receiver, requirements of both the dynamic range of sigma-delta modulator and the Q of analog filters are relaxed.

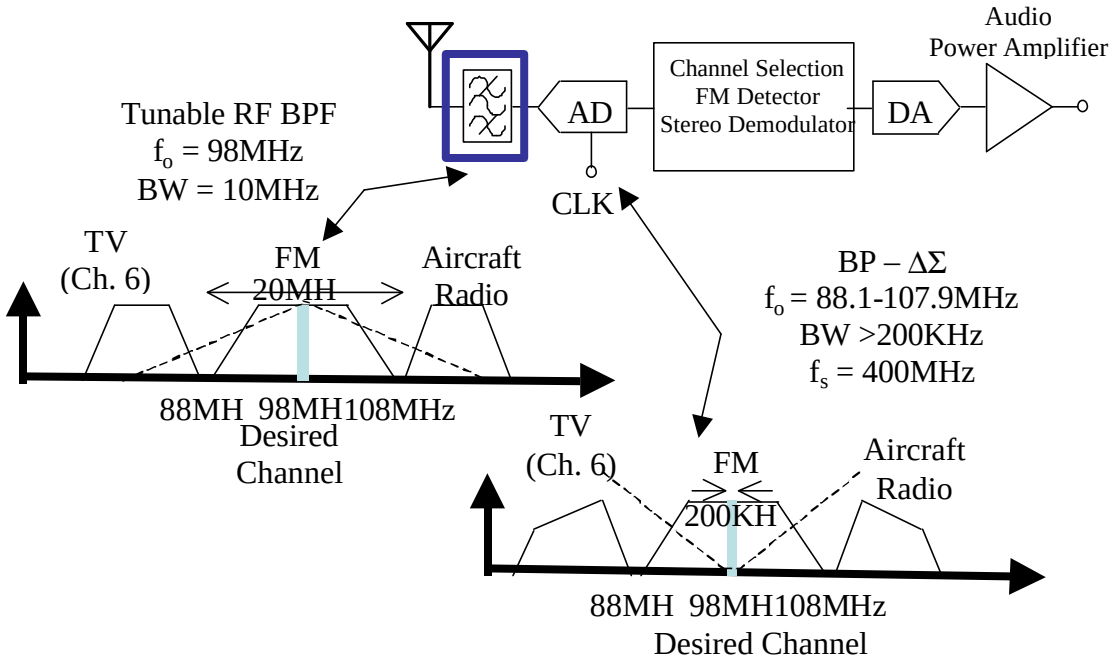


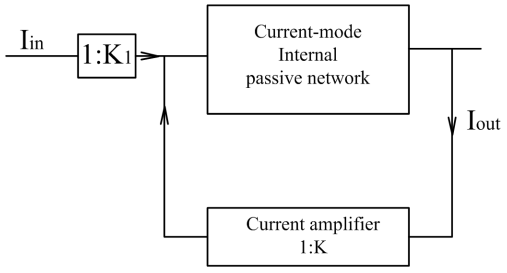
Figure 4.5 A novel FM front-end

4.2 A 100MHz RF low-noise and high-Q filter

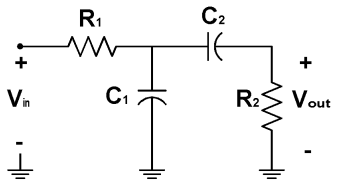
4.2.1 Block Diagram

As mentioned in chapter 3, both systems developed in this work adopt the architecture shown in Figure 3.10. The 100MHz RF low-noise and high-Q filter include the internal passive network and amplifiers. The system architecture is repeated in Figure 4.6(a) to better explain how the system is composed.

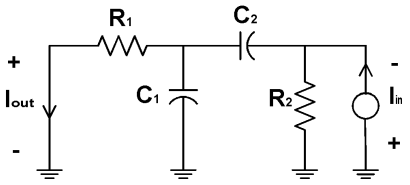
A voltage mode second order passive network with equal R's and equal C's is considered as the internal passive network. Voltage-mode to current-mode transformation is then used to convert the network into current-mode circuits as shown in Fig4.6(c).



(a)



(b)



(c)

Figure 4.6 (a) system architecture (b) voltage-mode internal passive network (c) current-mode internal passive network

The transfer function of the passive network shown in Figure4.6(c) is expressed as follows.

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\frac{1}{R_1C_1}}{\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2}} \cdot \frac{s\cdot(\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2})}{s^2+s\cdot(\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2})+\frac{1}{R_1R_2C_1C_2}} \quad (4.1)$$

Characteristic parameters are extracted from (4.1):

$$A_{IPN\_I} = \frac{\frac{1}{R_1C_1}}{\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2}}$$

$$w_{IPN\_I} = \sqrt{\frac{1}{R_1R_2C_1C_2}}$$

$$Q_{IPN\_I} = \frac{\sqrt{\frac{1}{R_1R_2C_1C_2}}}{\frac{1}{R_2C_1}+\frac{1}{R_1C_1}+\frac{1}{R_2C_2}}$$

Assuming that:

$$R_1 = R_2, C_1 = C_2$$

which gives:

$$A_{IPN\_I} = \frac{1}{3}$$

$$Q_{IPN\_I} = \frac{1}{3}$$

The transfer function of the overall system is:

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{K_1 \cdot \frac{1}{3} \cdot s \cdot \frac{w_{IPN\_I}}{1/3}}{s^2 + (1 - \frac{K}{3}) \cdot s \cdot \frac{w_{IPN\_I}}{1/3} + w_{IPN\_I}^2} \qquad (4.2)$$

Note from (4.2) that to achieve high Q values, the second term in the denominator of (4.2) must be very small and the gain of feedback amplifier, K, should be very close to 3.

4.2.2 Schematic Circuit

Although all of the major building blocks are designed in current-mode, it is usually favorable to have voltage input and output signals such that the system can easily interface with other voltage-mode systems.

At the input of system, voltage to current conversion is performed by a transconductor. At the output of system, a transimpedance stage is usually required to convert current into voltage. In this design, however, an output voltage is easily available by running the output current through a resistor in the internal passive network. A separate transimpedance stage is not necessary (illustrated in Figure 4.7).

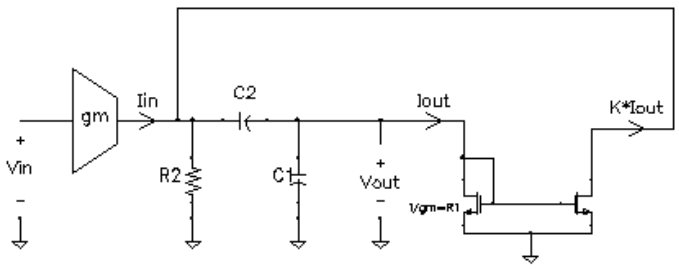


Figure 4.7 System diagram with voltage input/output

Considering matching issues, resistors in the internal passive network are realized by 1/gm of a revised version of diode connected transistors. The current amplifier in the feedback path is realized by the tunable wide swing cascode current amplifier as shown in Figure 3.16.

A simplified schematic of the current mode filter with voltage input and output signal is shown in Figure 4.8.

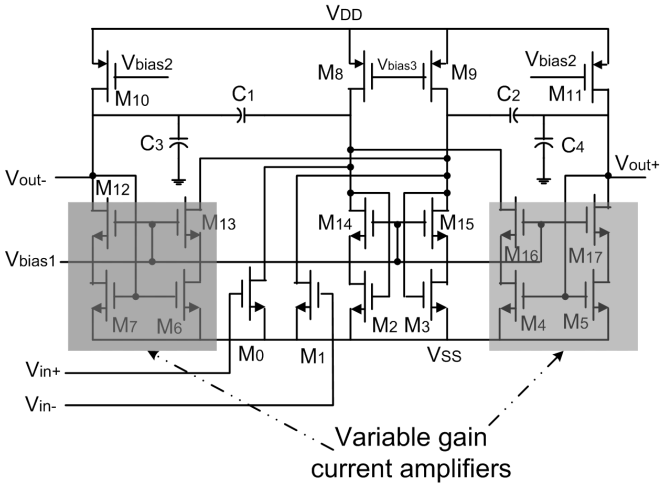


Figure 4.8 A simplified schematic of the current mode filter with voltage input and output

Figure 4.8 shows a differential version of the 100MHz RF low-noise and high Q filter. The input transistors M_0 and M_1 convert input voltages into currents. Looking into drain of M_{14} & M_{15}, the equivalent resistance is $1/g_{m2}$, and $1/g_{m3}$, respectively. Also looking into drain of M_{12} and M_{17}, the equivalent resistance is $1/g_{m7}$, and $1/g_{m5}$, respectively. If a mapping is built between Figure 4.8 and the block diagram shown in Figure 4.6, we can see that:

$$R_1 = \frac{1}{g_{m5}} = \frac{1}{g_{m7}}$$

$$R_2 = \frac{1}{g_{m2}} = \frac{1}{g_{m3}}$$

Two shaded areas in Figure4.8 represent variable gain current amplifiers as shown in Figure 3.16. For ease of discussion, switches and controls for the variable gain amplifier are omitted. M_{13}, M_6, M_{16}, and M_4 are used to represent sums of switch-controlled and binary weighted transistors. Common-mode feedback circuits and bias circuits are ignored in Figure 4.8 for ease of discussions.

4.3 Performance Analysis

4.3.1 Parasitic Analysis

Parasitic capacitance and resistance create unwanted poles and limit the frequency range over which the system can operate properly. Influences of parasitic capacitance are generally unavoidable since large aspect ratio and long channel devices are usually required for good matching and noise performance. It is desirable to reduce parasitic resistance such that all parasitic poles are at much higher frequencies than the working frequencies.

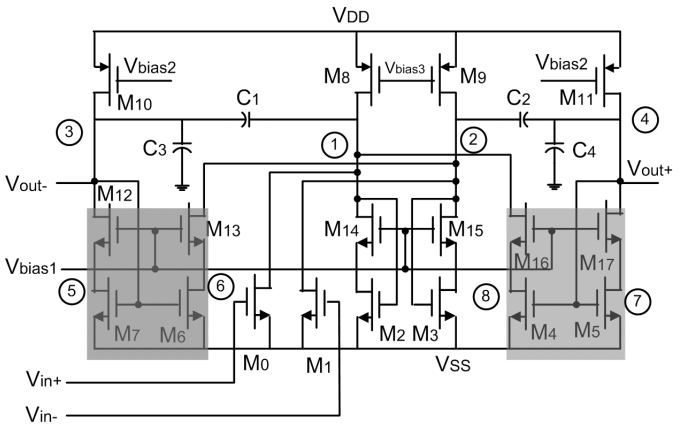


Figure 4.9 a simplified schematic of 100MHz RF low-noise and high-Q filter with node labels

Figure 4.9 shows a simplified schematic of 100MHz RF low-noise and high-Q filter with node labels. Common-mode feedback circuitry is not shown since the parasitic pole frequencies of CMFB circuits are much higher than the working frequencies of the main circuitry. From Figure 4.9, we can see that there are six "internal nodes" in the circuit, labeled ① ②, and ⑤ - ？. Also there are two output nodes, labeled ③ and ④.

The impedance looking into node ① can be calculated as:

$$r_{(1)} = r_{ds1} // r_{ds8} // \frac{r_{ds14} + r_{ds2} + g_{m14} r_{ds14} r_{ds2}}{g_{m2} r_{ds2} + g_{m14} g_{m2} r_{ds14} r_{ds2}} // g_{m16} r_{ds16} r_{ds4} \approx \frac{1}{g_{m2}} \tag{4.3}$$

Similarly, we can calculate the impedance looking into node ②:

$$r_{(2)} \approx \frac{1}{g_{m3}} \tag{4.4}$$

Also, we can find impedance looking into node ③ and ④:

$$r_{(3)} \approx \frac{1}{g_{m7}} \qquad r_{(4)} \approx \frac{1}{g_{m5}} \tag{4.5}$$

The impedance looking into node ⑤ can be calculated as:

$$r_{(5)} = \frac{1}{g_{m12}} // r_{ds7} // r_{ds12} \approx \frac{1}{g_{m12}} \tag{4.6}$$

Similarly impedances looking into nodes ? - ? are found as:

$$r_{(6)} \approx \frac{1}{g_{13}} \qquad r_{(7)} \approx \frac{1}{g_{m17}} \qquad r_{(8)} \approx \frac{1}{g_{m16}} \tag{4.7}$$

Note from (4.3)~(4.7) that all circuit nodes are low impedance nodes, which implies that all parasitic poles and zeros of the system are much higher than operation frequencies of the system.

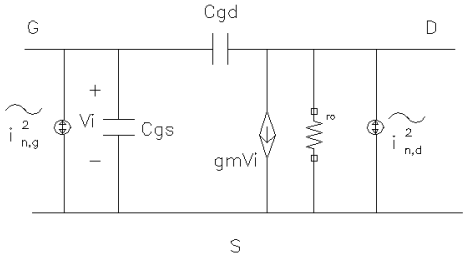


Figure 4.10 MOSFET small signal model with equivalent noise generators

4.3.2 Noise Analysis

The noise of the MOSFET can be represented by equivalent noise generators $\tilde{i}^2_{n,g}$ and $\tilde{i}^2_{n,d}$ in Figure 4.10 [53]. The channel thermal noise, the major source of MOSFET noise, and the channel flicker noise, are represented by a noise current generator, $\tilde{i}^2_{n,d}$, connected between the source and the drain. The noise generated by the gate leakage current is represented by $\tilde{i}^2_{n,g}$, and becomes significant only when the source impedance that drives the gate becomes very large. The noise generators shown in

Figure 4.10 are all independent of each other. When a MOSFET operates in the saturation region, the values of $\tilde{i}_{n,g}^2$ and $\tilde{i}_{n,d}^2$ are

$$\tilde{i}_{n,g}^2 = 2qI_G\Delta f \ , \tag{4.8}$$

$$\tilde{i}_{n,d}^2 = 4kT\left(\frac{2}{3}g_m\right)\Delta f + K_f\frac{I_D^a}{f}\Delta f \ , \tag{4.9}$$

where I_G is the gate leakage current, K_f is a constant for a given device, and a is a constant between 0.5 and 2.

For high frequency applications such as the FM radio receiver, effects of flicker noise can be ignored. We also ignore the effect of noise generated by the gate leakage current since the magnitude is much smaller than the channel thermal noise.

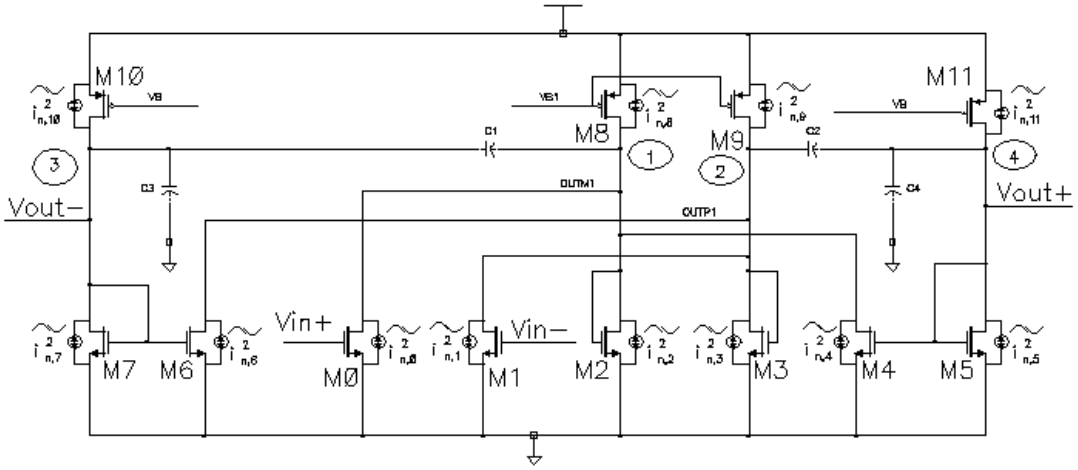


Figure 4.11 a simplified schematic for noise analysis

A simplified schematic is drawn in Figure 4.11. It can be proved that the noise generated by cascode transistors M_{12}~M_{17} contribute very insignificantly to the overall noise performance (Appendix A), thus they are removed for simplicity of noise analysis. Simulation results showed that removal of cascode transistors wouldn't change the results of noise analysis.

In Figure 4.11, channel thermal noise sources of MOSFETs are represented by noise current generators $\tilde{i}_{n,l}^2 (l = 1,2,...,11)$. Assume all noise generators are independent of each other. The values of $\tilde{i}_{n,l}^2 (l = 1,2,...,11)$ are

$$\tilde{i}_{n,l}^2 = 4kT\left(\frac{2}{3} g_{ml}\right)\Delta f \ , \tag{4.10}$$

where g_{ml} is the transconductance of M_l.

The equivalent input noise includes two parts: one is determined by the noise current through nodes ① and ? divided by *gm* of input transistors M_0 and M_1, the other is determined by the noise current through nodes ③ and ④ divided by the gain from input to nodes ③ and ④. As mentioned above, all noise generators are independent of each other. We can first assume all transistors directly connected to nodes ①and ? are noisy and the rest of the circuit noiseless, and calculate the first part of the equivalent input noise. Then we can assume all transistors directly connected to nodes ③ and ④ are noisy and the rest of the circuit noiseless, and calculate the second part of the equivalent input noise. The total equivalent input noise is the sum of the two parts of equivalent input noises.

A “half-circuit” is analyzed here to reveal the relationship between noise and gms of transistors. The noise current through node ① is the sum of the channel noise currents of M_0, M_2, M_4, M_8, and the noise current through node ③ is the sum of the channel noise currents of M_7, M_{10}. The value of noise current through node ① is

$$\tilde{i}^2_{n,(1)} = 4kT\frac{2}{3}(g_{m0} + g_{m2} + g_{m4} + g_{m8})\Delta f \ . \tag{4.11}$$

The first part of the equivalent input noise voltage is

$$\tilde{V}^2_{in,n,part1} = \frac{\tilde{i}^2_{n,(1)}}{g^2_{m0}} = 4kT\frac{2}{3}(\frac{1}{g_{m0}})\Delta f + 4kT\frac{2}{3}\frac{g_{m2} + g_{m4} + g_{m8}}{g^2_{m0}}\Delta f \ . \tag{4.12}$$

The value of the noise current through node ③ is

$$\tilde{i}^2_{n,(3)} = 4kT\frac{2}{3}(g_{m7} + g_{m10})\Delta f \ . \tag{4.13}$$

Figure 4.12 illustrates how the second part of input noise can be calculated from the noise current that flows through node ③.

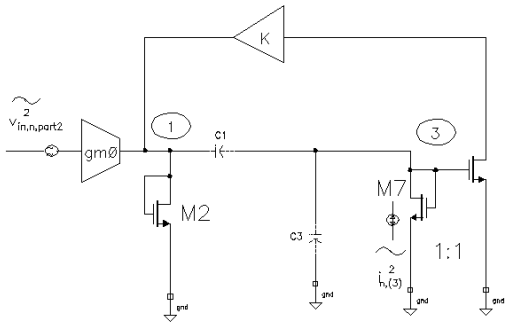


Figure 4.12 Illustration of how to calculate the second part of equivalent input noise

Assume $g_{m2} = g_{m7}, C_1 = C_3$. The value of the second part of the equivalent input noise is

$$\tilde{V}^2_{in,n,part2} = \frac{\tilde{i}^2_{n,(3)}}{\left| \frac{g_{m0} s \frac{g_{m2,7}}{C_{1,3}}}{s^2 + (3-K) s \frac{g_{m2,7}}{C_{1,3}} + \frac{g^2_{m2,7}}{C^2_{1,3}}} \right|^2} = 4kT \frac{2}{3} \frac{g_{m7} + g_{m10}}{g^2_{m0}} (3-K)^2 \Delta f \Big|_{s=j\frac{g_{m2,7}}{C_{1,3}}} \tag{4.14}$$

The value of K is designed to be close to 3 such that the filter Q can be enhanced to the desired value, (3–K) that is much less than 1. Therefore, the effect of the second part of the equivalent input noise is insignificant as compared to the first part. The total equivalent input noise is mainly determined by the first part. To achieve a low equivalent input noise, large g_m values are required for M_0, M_1. At the same time, to keep noise low, small g_m values are desirable for M_2, M_3, M_4, M_6, M_8 and M_9.

4.4 Simulation Results

Cadence simulations are performed on the 100MHz RF low-noise and high Q filter. All components are modeled based on NSC CMOS9 library. A schematic of the test circuit is shown in Figure 4.13. Two 25O resistors are connected to differential input terminals to match a 50O input source. Large isolation capacitors are in series with the matching resistors such that they will not affect the DC biasing of the circuit. The 25O matching resistors are implemented by on-chip poly resistors, while the isolation capacitors have to stay off-chip due to their large capacitance values.

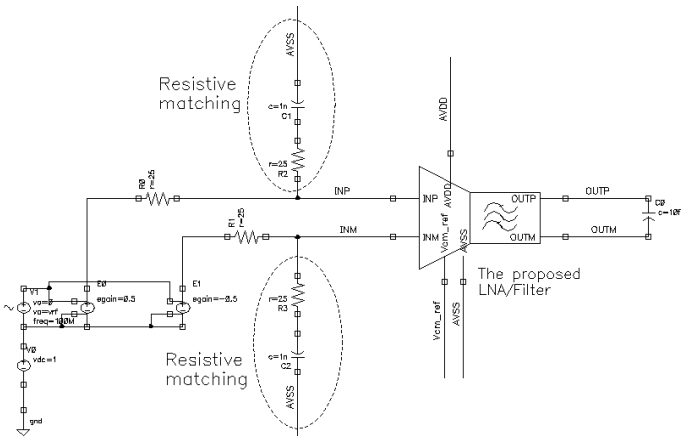


Figure 4.13 a schematic of the test circuit

- AC response

A typical AC response is shown in Figure 4.14. The AC characteristic values are listed in Table 4.2.

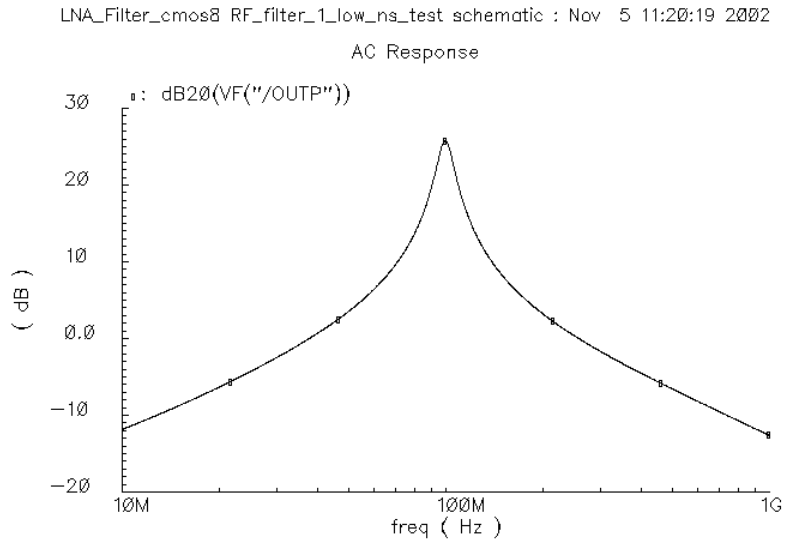


Figure 4.14. A typical AC response

Table 4.4. AC characteristics

f_0 (MHz)	100.2
Mid-band Gain (dB)	25.69
3-dB frequencies	94.1 & 105.2
Bandwidth	11.1
Q	9

Theoretically, the Q value of the circuit can be adjusted from less than 1 to infinity. However, as Q increases, the mid-band gain also increases proportionally, which results in reduced IP3 and dynamic range. A practical range of Q is from 5 to around 20.

The simulations result of AC responses with different Q is shown in Figure 4.15.

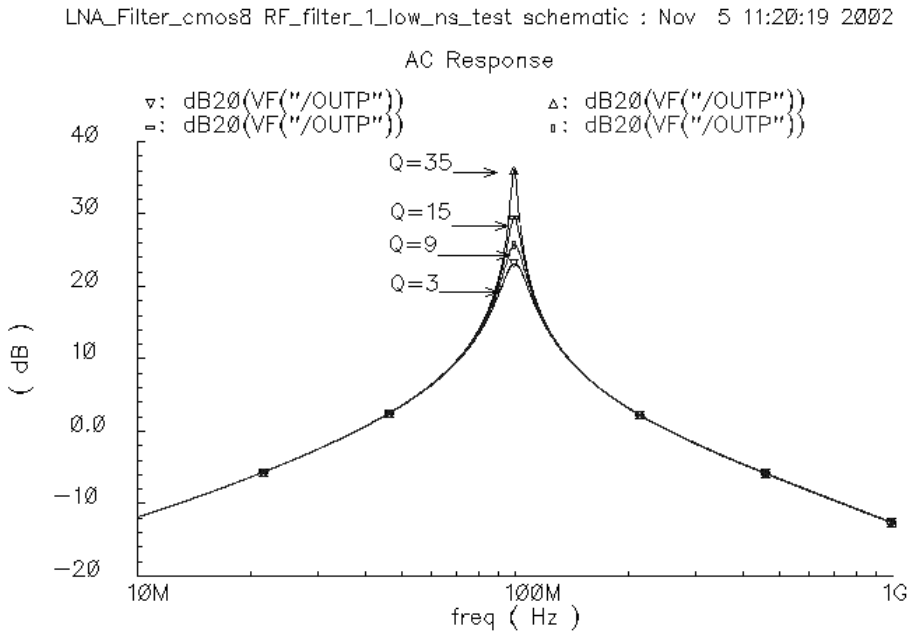


Figure 4.15 The AC response with different Q

The Q tuning resolution depends on sizes of transistor arrays, the g_m's of which determine the gains of feedback current amplifiers. An n-bit digitally controlled transistor array yields $2^n - 1$ different gm values, and $2^n - 1$ different Q values.

- Noise

Noise performance is evaluated by the equivalent input noise as shown in Figure 4.16. The equivalent input noise at 100MHz is $5.68nV/\sqrt{Hz}$. Noise floor is calculated by integration. The integration interval is from 97MHz to 103MHz which is $\frac{p}{2}$ times the 3dB bandwidth. The noise figure value from the above calculation is 9.0dB. Cadence noise figure simulation results are shown in Figure 4.17. The noise figure is 9.3dB at 100MHz from the plot.

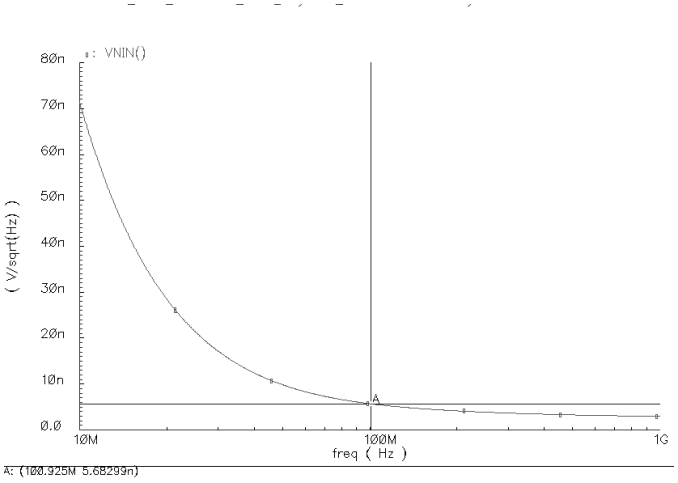


Figure 4.16 Equivalent input noise

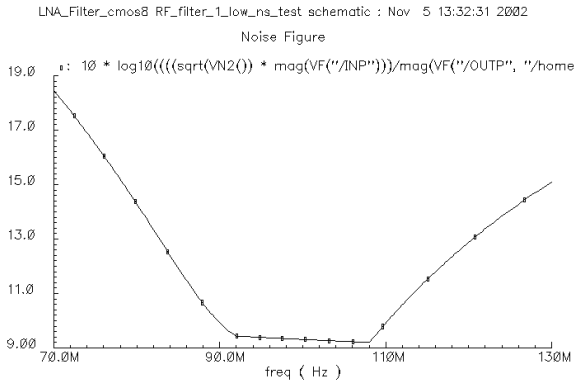


Figure 4.17 Noise figure

The minimum requirement of SNR at RF input is 26dB for FM receivers [42-43]. Since the input is matched to a 50O source, the RF sensitivity is then determined by the following equation:

$$P_{RF,sensitivity} = -174dbm/\sqrt{Hz} + 10\log B + NF + SNR_{\min},$$

where B is chosen to be 15 KHz for the worst case calculations as suggested in [42-43]. To obtain 26dB SNR at RF input, the RF sensitivity (minimum detectable RF signal voltage with required SNR) is **3.15uV**. The minimum detectable RF power is **-97dbm**.

- Linearity

The 1dB compression point of the proposed circuit is **–36.05** dBm as shown in Figure 4.18. This can be improved by increasing the gate overdrive voltage, V_{GST}, of critical transistors. However, to keep the same noise performance, more currents are consumed to keep g_m values constant while increasing V_{GST}.

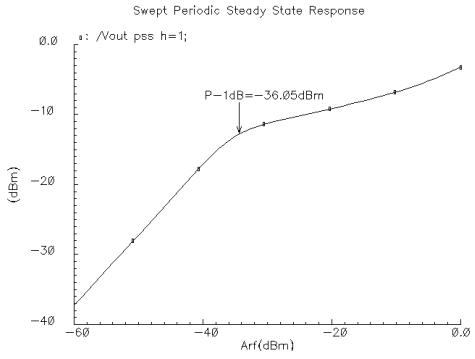


Figure 4.18 1dB compression point

Dynamic range is the ratio of the maximum signal level that a circuit processes with an acceptable amount of distortion to the minimum detectable signal level. There are several ways to numerically define the value of dynamic range for a circuit, such as Spurious Free Dynamic Range (SFDR) and 1-dB compression Dynamic range (1-dB DR).

This work adopts the 1-dB DR definition such that the result is comparable to similar works [64]:

$$DR = P_{1-dB} - Noise\_floor = 48.3dB$$

- Distortion

Simulation result of a two-tone test is shown in Figure 4.19. Frequencies of the two test tones are 98MHz and 102MHz. The input signal level is 1mV (–46.9dBm), and the magnitude of IM3 is **32.1**dB less than the fundamental tones.

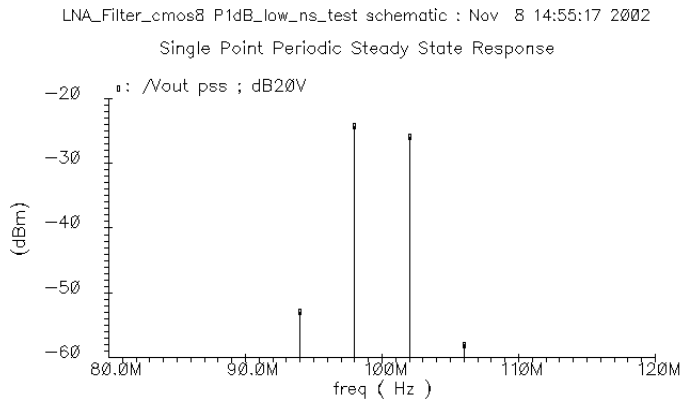


Figure 4.19 Two-tone test simulation result

Figure 4.20 shows the output harmonics of a single test tone at 100MHz. The magnitude of the input test tone is 1mV. The y-axis of Figure 4.20 is scaled by the input signal magnitude and then converted into dB. The total harmonic distortion is 0.1%.

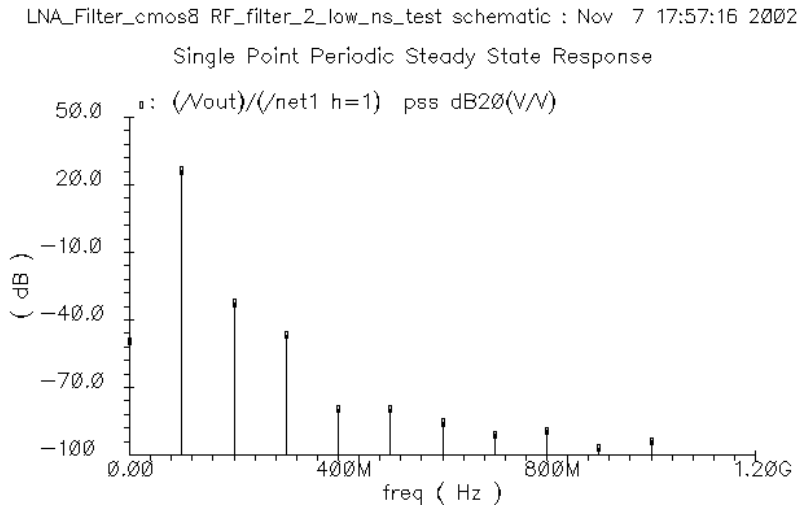


Figure 4.20 Harmonic distortion simulation result

4.5 Tuning Schemes

Tuning circuits are designed to compensate for environment and process variations. When the 100MHz filter is used as part of an FM radio front end as shown in Figure 4.5, it performs 'partial-band selection', and the passband of the filter should cover a desired signal channel and some adjacent channels. The requirements on tuning accuracy are greatly relaxed since the desired signal channel only occupies a small fraction of the passband. The filter performs correctly as long as the desired signal channel stays in the passband, regardless of center frequency and bandwidth. Switched arrays providing discrete tuning are good enough for these applications.

4.5.1 Frequency Tuning

As described earlier, the 100MHz low-noise high-Q filter is designed to select a portion of the FM band instead of a single channel or a whole band, which results in a

relaxed requirement on the accuracy of center frequency tuning. Very good accuracy must be achieved for tuning of channel-selection filters, such that the desired channel is not missed. In this work, since the pass-band covers tens of channels, moderate tuning accuracy is enough to ensure that the desired channel is one of them.

Center frequency tuning of integrated filters is usually done by varying the value of gm by adjusting the DC bias current. This is difficult since the center frequency is determined by $w_0 = \frac{g_m}{C}$. Center frequency tuning is accomplished by varying the value of C. Switched capacitor arrays are used to change the value of C. The array contains two types of components: fixed and switched capacitors. The fixed capacitance is represented by C_{fixed} in Figure 4.21, and the switched capacitors are represented by C_0's in Figure 4.21. The value of the fixed capacitance should be small enough such that its capacitance will not be larger than the desired worst case value. At the same time, it should be as large as possible so that too many switched capacitors are not needed.

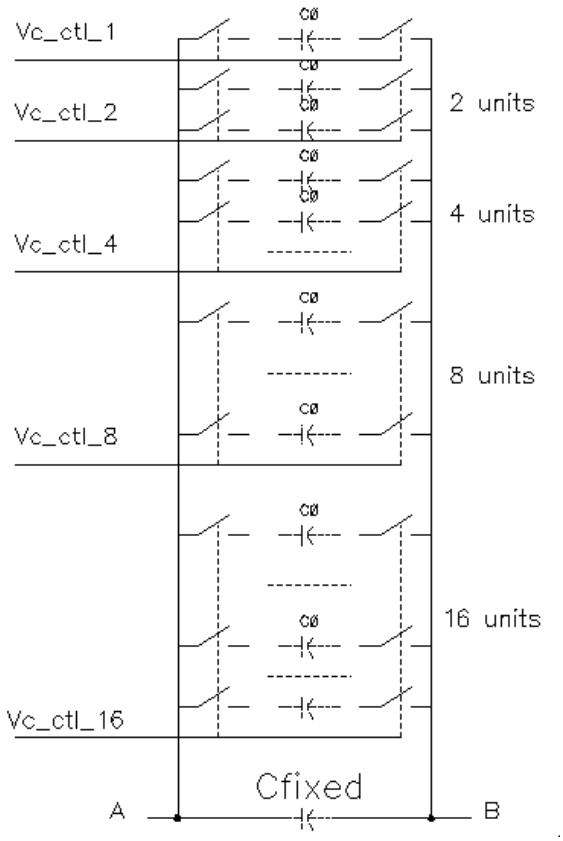


Figure 4.21 A binary-weighted cap-array

The capacitor array is binary weighted. The value of switched capacitance can be controlled as $nC_0, n = 1,2,.....,31$. The switch circuitry is shown in Figure 4.22.

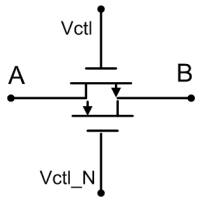


Figure 4.22 A transmission gate switch

The effect of switch resistance must be taken into account even though large devices are used to reduce it. Recall from Chapter 3 of this report, the Q and gain of the

circuit are determined by those of the internal second-order RC band-pass network, and the gain of a current amplifier, K. The value of K is chosen such that the product of K and the pass-band gain of the internal passive network, A_{IPN}, is close to 1. Taking into account the effect of switch resistance, both gain and Q of the internal band-pass network are reduced. Therefore, a larger K is required to keep the product of K and A_{IPN} close to 1. The current amplifiers are implemented using current mirrors, therefore the power consumption of the current amplifiers increase as their gain, K, increases.

4.5.2 Q Tuning

As mentioned previously, the Q of the filter is determined by Q_{IPN}, A_{IPN} and *K*. The Q tuning is implemented by adjusting *K*, the gain of the feedback current amplifier (two lower shaded areas in Figure 4.23).

Variable gain current amplifiers (Figure 3.16) are used to change the gain in the feedback path. Current gains are controlled by switches and binary weighted W/L's. When digital control signals are applied to switches S0~S5, gain of the current amplifier varies from 2 to 4, at a resolution of 0.03125. There are 64 steps of increments from 2 to 4, with a step size of 0.03125. The gain will be one of the 64 discrete values. A small step size is chosen since the Q of the overall system is sensitive to the gain of current amplifier especially as the Q value is large.

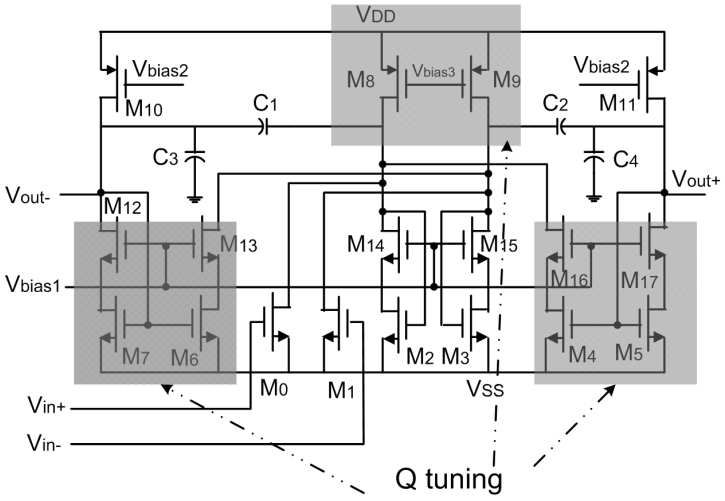


Figure 4.23. A simplified schematic with Q tuning

Table 4.3 Design parameters of variable gain current amplifiers

S5	S4	S3	S2	S1	S0	Bias current	Current gain
0	0	0	0	0	0	0.6mA	2
0	0	0	0	0	1	0.6375mA	2.03125
0	0	0	0	1	0	0.675mA	2.0625
0	0	0	1	0	0	0.75mA	2.125
0	0	1	0	0	0	0.9mA	2.25
0	1	0	0	0	0	1.2mA	2.5
1	0	0	0	0	0	1.8mA	3

DC bias currents vary as transistors are switched in/out of the variable gain current amplifiers. Switched PMOS transistors (upper shaded area in Figure 4.23) are designed to accommodate changing bias currents such that common mode voltages at internal and output nodes are stabilized. Figure 4.24 illustrates the PMOS bias circuit.

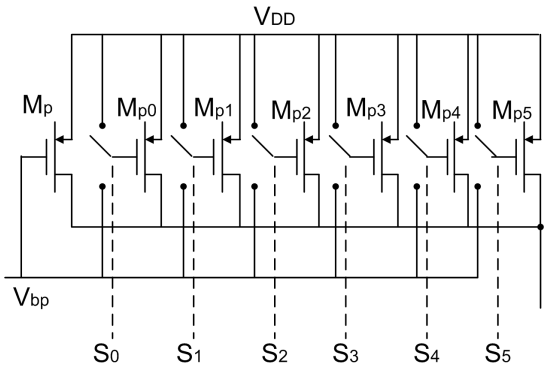


Figure 4.24 Switched PMOS bias circuit

4.6 Layout of the 100MHz Low-noise High-Q Filter

4.6.1 Layout of Capacitor Arrays

There are two capacitors in the prototype internal passive network (Figure 4.6 (c)), C_1 and C_2. At the beginning values of C_1 and C_2 are both designed as 4pF, and implemented using poly-poly capacitors provided by NSC 0.18um CMOS processes. A poly-poly capacitor is composed by two poly plates in parallel, the parasitic capacitances between bottom plane and substrate are generally 20% of the desired capacitance values. Note that the parasitic capacitor C_2 is in parallel with C_1, thus C_1 is designed to be 3.2pF to 'absorb' the parasitic capacitance generated by C_2.

The layout of capacitors is shown in Figure 4.25. Two common centroid capacitor arrays are laid out for high accuracy matching. In the top array are two 3.2pF capacitors laid out in two rows and four columns, unit capacitance value is 0.8pF. In the bottom array are two 4.0pF capacitors, also laid out in two rows and four columns. The unit capacitance value is 1.0pF. With two by four arrays, the matching error between capacitive loads seen from the differential nodes is less than 1%.

Dummy capacitors are placed around the array to equalize peripheral effects. Extra cautions are taken when layout interconnection wires, size of wires are also matched to an extent such that matching errors between differential capacitance loads are minimized.

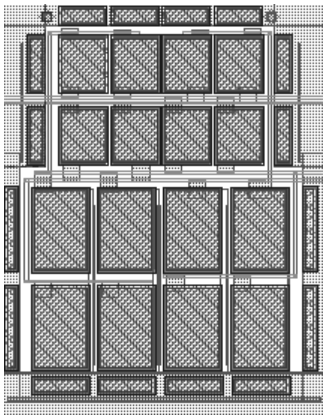


Figure 4.25 Layout of cap array

4.6.2 Layout of the Variable Gain Current Amplifiers

Variable gain current amplifiers are designed to precisely control Q value of the filter. Two such amplifiers are required for differential operation. Gains of these two amplifiers must be matched such that even order harmonics are minimized. To achieve good matching, transistors are split and laid out as arrays and common centroid techniques are used to maximize matching between gains of the two amplifiers. A fraction of the layout of variable gain amplifier is shown in Figure 4.26. The upper 8 transistors (transistors controlled by S4 in Figure 3.16) form one switched path in the

variable gain amplifiers; the lower 8 transistors (transistors controlled by S3 in Figure 3.16) form another path.

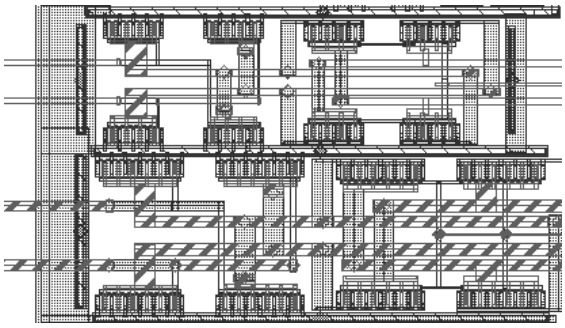
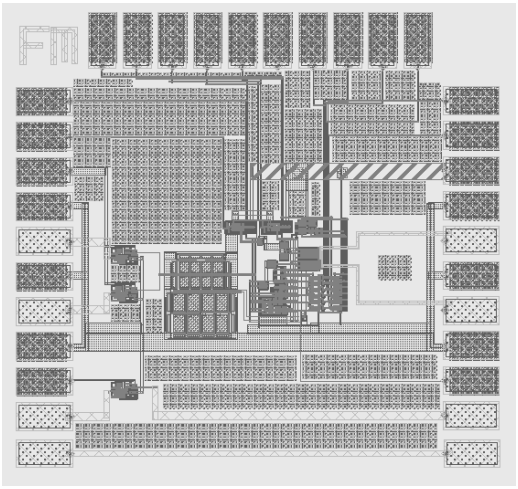


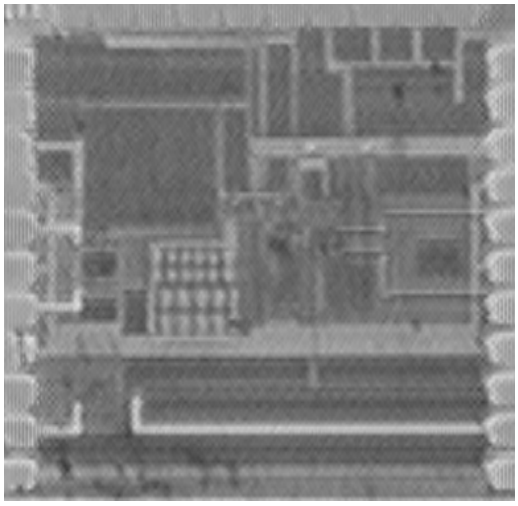
Figure 4.26 Layout of transistor arrays

4.6.3 Layout of the Final Design

A test layout is shown in Figure 4.27(a). Voltage buffers are designed and connected to output of the main circuits, to drive capacitive load of bonding pads, and also the capacitive loads of measurement equipment. Each buffer consumes around 1mA DC current. A die photo is shown in Figure 4.27(b)



(a)



(b)

Figure 4.27 (a) Layout of a 100MHz RF low-noise high-Q filter (b) die photo

4.7 Experiment Results

4.7.1 Test System Setup

The 100MHz RF low-noise and high-Q filter is fabricated through the NSC 0.18um CMOS process. Measurements are performed by probing bare dies using three

groups of probe arrays (Figure 4.28). A 10-access DC probe is placed above the DUT to provide DC bias and control signals; a 10-access RF/DC probe is placed on right and left side of the DUT to provide RF accesses and additional DC accesses.

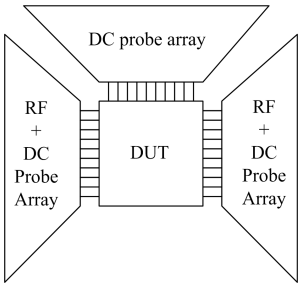


Figure 4.28 Measurement setup

A test PCB is designed to facilitate interfacing between probes and equipment. The diagram of test PCB is shown in Figure 4.29(a), photo of test PCB is shown in Figure 4.29(b).

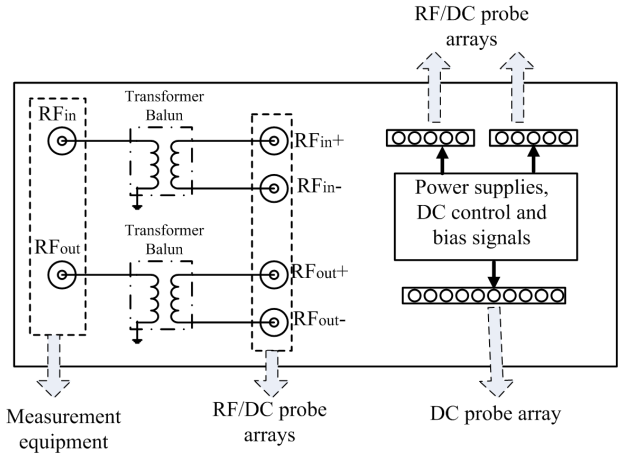


Figure 4.29 (a) Diagram of test PCB

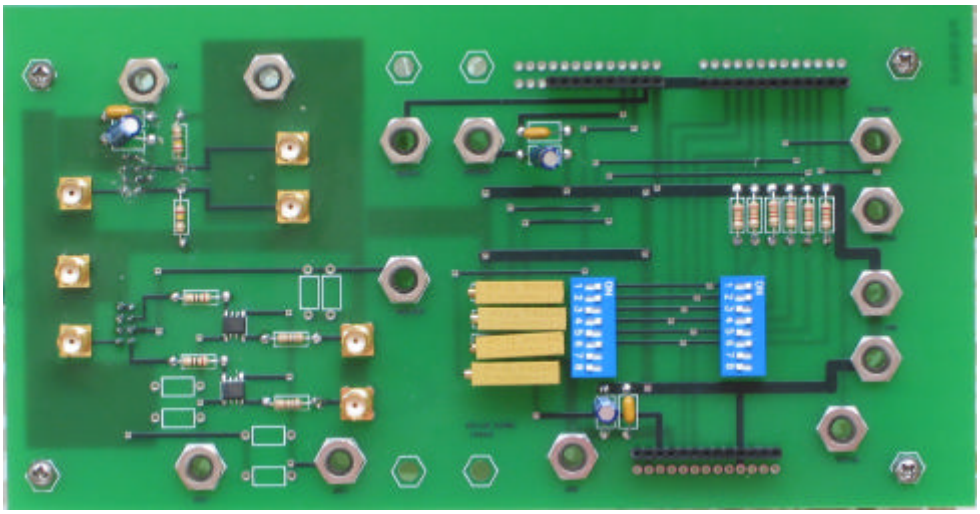


Figure 4.29 (b) Photo of test PCB

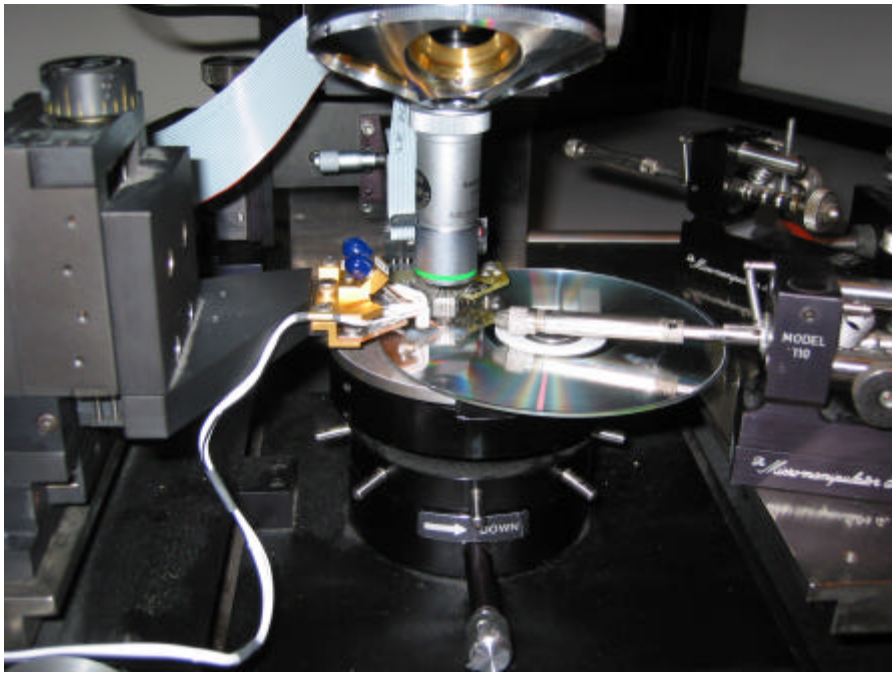


Figure 4.30 Measurement setup

At the beginning of measurement, all test equipments are calibrated. DC operation point was checked and verified before ac signals were applied to the circuit.

4.7.2 Measurement of Frequency Responses

Frequency response of the 100MHz design is measured using a network analyzer and a tunable wideband attenuator. The attenuator helps to set the amplitude of RF input signals to DUT to 1mV (-47dBm), which resides in the middle of the dynamic range. Frequency response measurement setup is shown in Figure 4.31.

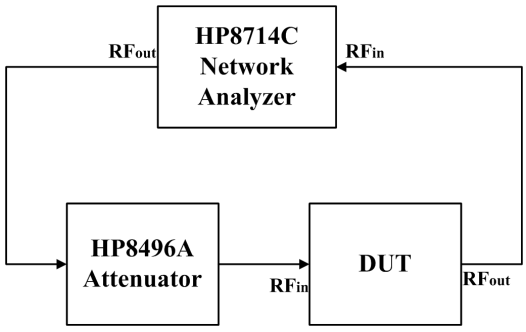


Figure 4.31 Frequency response measurement setup

Effects of the attenuator and transformer baluns are measured separately and de-embedded from the overall measured frequency response. Losses through cables and probes are measured using an on-chip straight through path, the results is shown in Figure 4.32. We can see that there is around 0.5dB loss caused by cables and lossy contacts between probes and metal pads on wafer.

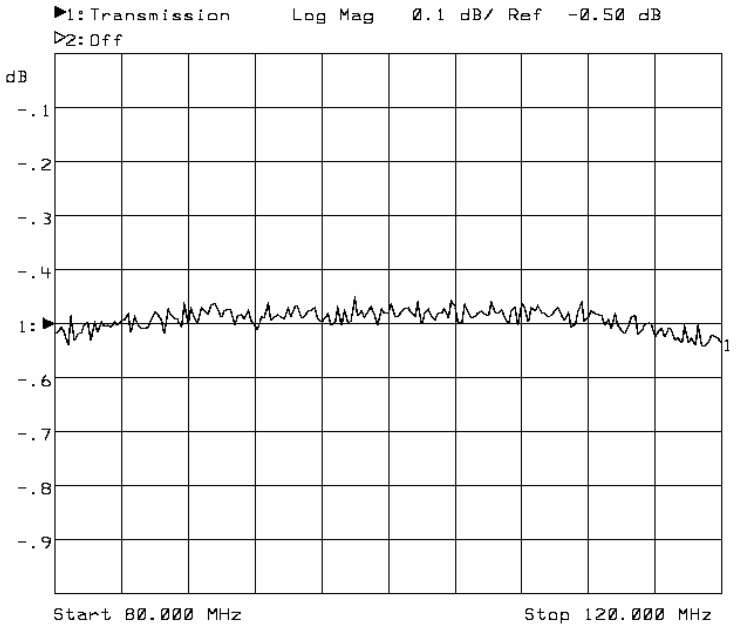


Figure 4.32 Measurement of losses through cables and probes

Recall from section 4.2, Q of the 100MHz filter is controlled by the gain in the positive feedback path, which is binarily varied by a group of external control signals. When all of the control signals are set to 0, the gain of the positive feedback is minimized, as well as the total DC current flowing through the circuit. A measured frequency response when all of the control signals are set to 0 (total current 4.8mA) is shown in Figure 4.33.

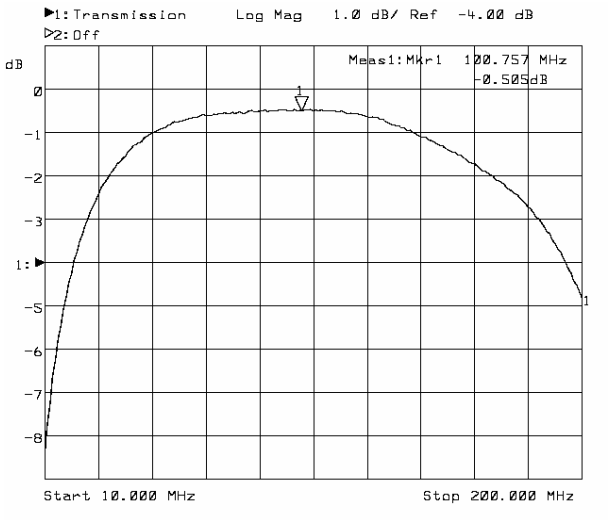


Figure 4.33 Measured frequency response when
all external gain-control signals are set to 0

As the gain in the positive feedback path increases, the Q of the 100MHz filter is boosted, a measured frequency response of Q=28.9 is shown in Figure 4.34. The total DC bias current is increased to 9.9mA.

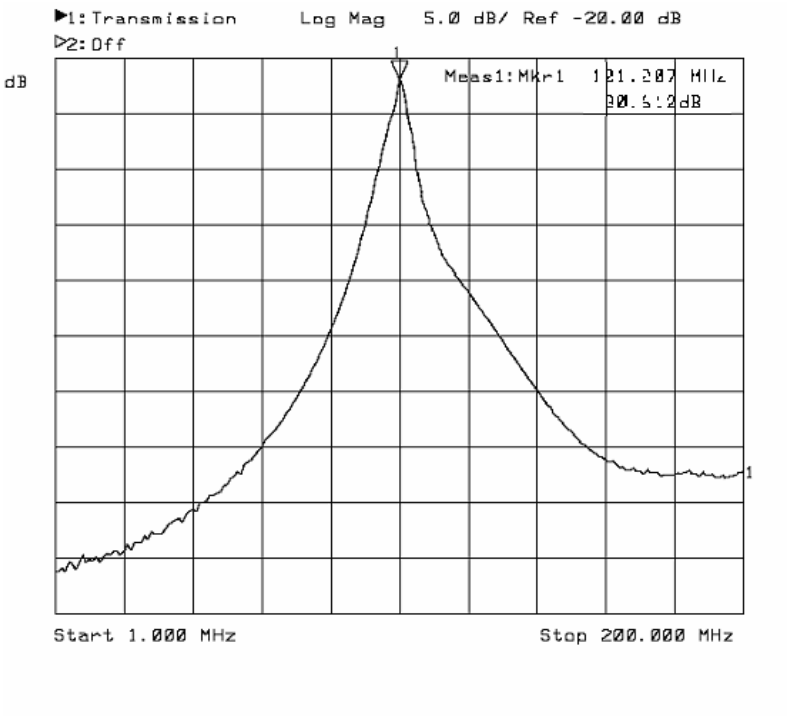


Figure 4.34 (a) Frequency response

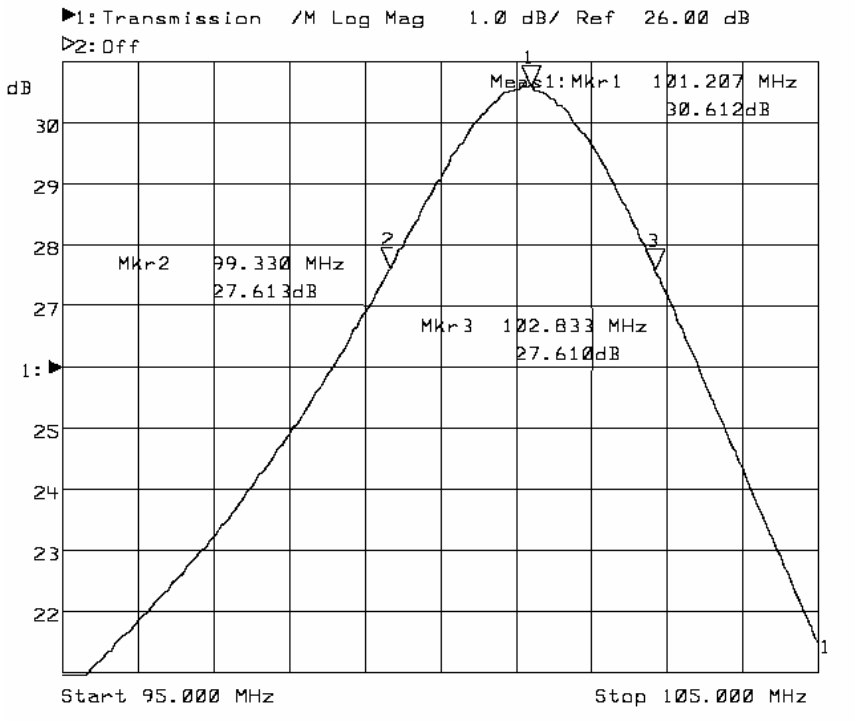


Figure 4.34 (b) Frequency response with marker 1

Another way to measure frequency responses is to manually sweep the frequency of input signals, and measure the amplitudes of output waveforms using an oscilloscope (Figure 4.35). Frequency responses are obtained by extrapolating from the discrete measurement data.

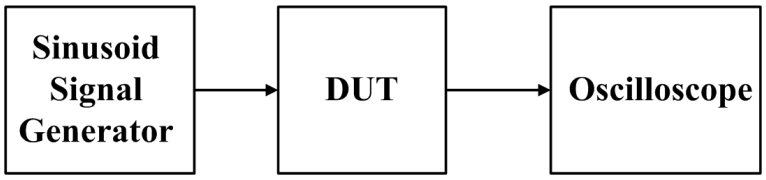


Figure 4.35 Measuring frequency responses using signal generator and oscilloscope

Transient responses are measured by applying sinusoid signals to the input of the 100MHz circuit, with frequencies vary from 90MHz to 110MHz, at 1MHz intervals. Extra data points are added for accurate measurement at around the center frequency (peak). Figure 4.36 shows an example of transient response when frequency of the input tone is 102MHz.

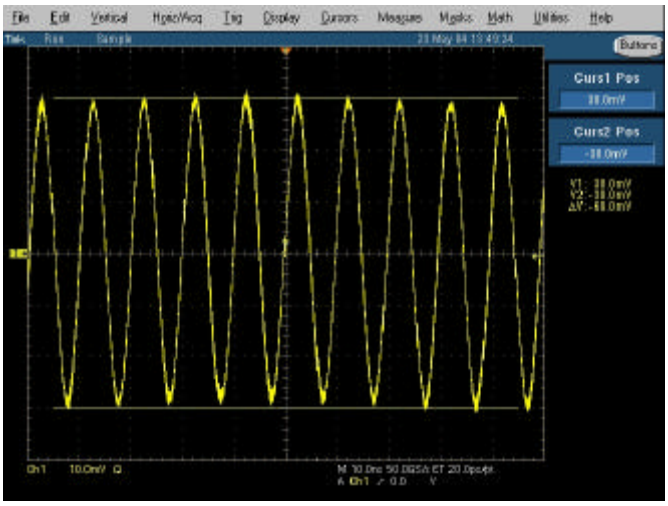


Figure 4.36 Output waveform measured by oscilloscope

4.7.3 Noise Measurement

As shown in Figure 4.16, the input equivalent noise at 100MHz is 5.68 $nV/\sqrt{Hz}$. The concept of 'input referred noise' is a fictitious quantity for fair comparisons of noise performance regardless of the transfer characteristics function of specific systems. In general, the output noise spectrum density is measured to verify noise performance of a design.

In this work, noise measurement is performed using a Rohde & Schwarz spectrum analyzer FSU8, a diagram of noise measurement setup is shown in Figure 4.37. The output noise of the 100MHz circuit is measured when RF input is connected to AC ground (DC wise both RF inputs are connected to Vin_cm, the input common-mode voltage). Equivalent input noise is derived by dividing output noise by gain of the circuit. When the spectrum analyzer is configured for noise measurement, its resolution bandwidth, video bandwidth and sweep time are carefully defined such that the noise of

the spectrum analyzer itself is minimized and the noise floor of the equipment is well below that of the test circuit.

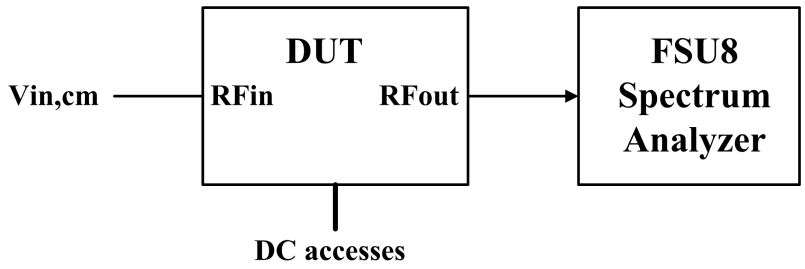
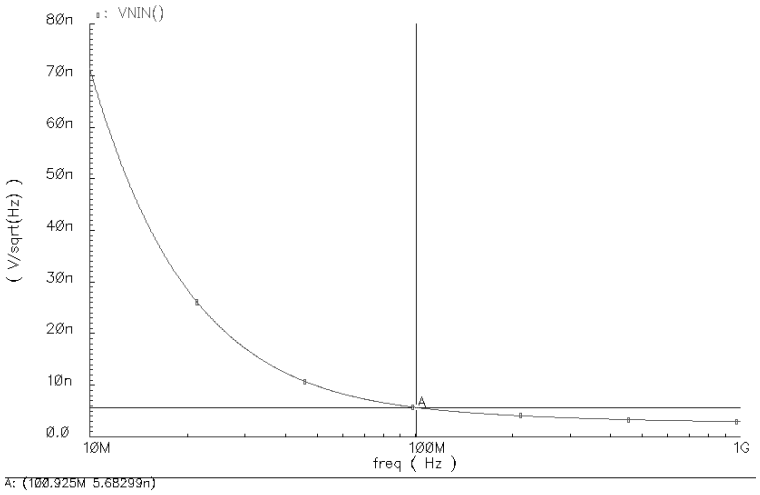
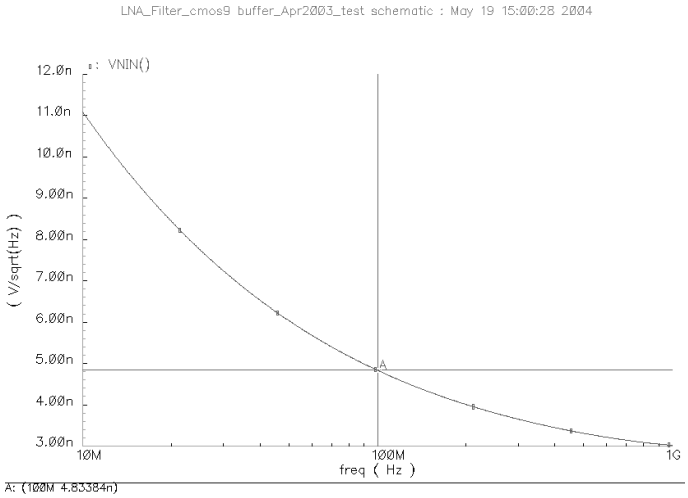


Figure 4.37 Noise measurement setup

Note that a buffer is loaded at each of the differential output terminals. Thus the measured output noise contains noise generated by both the main circuitry and the buffers. To identify noise generated from the 100MHz filter circuit, recall the noise simulation results (Figure 4.38). Shown in Figure 4.38(a) is the equivalent input noise of the 100MHz filter, and in Figure 4.38(b) is the equivalent input noise of a buffer. We can see that the equivalent input referred noise spectrum of a buffer is $4.84\,nv/\sqrt{Hz}$ at 100MHz.



(a) the equivalent input noise of the 100MHz filter



(b) the equivalent input noise of a buffer

Figure 4.38 Equivalent input noise

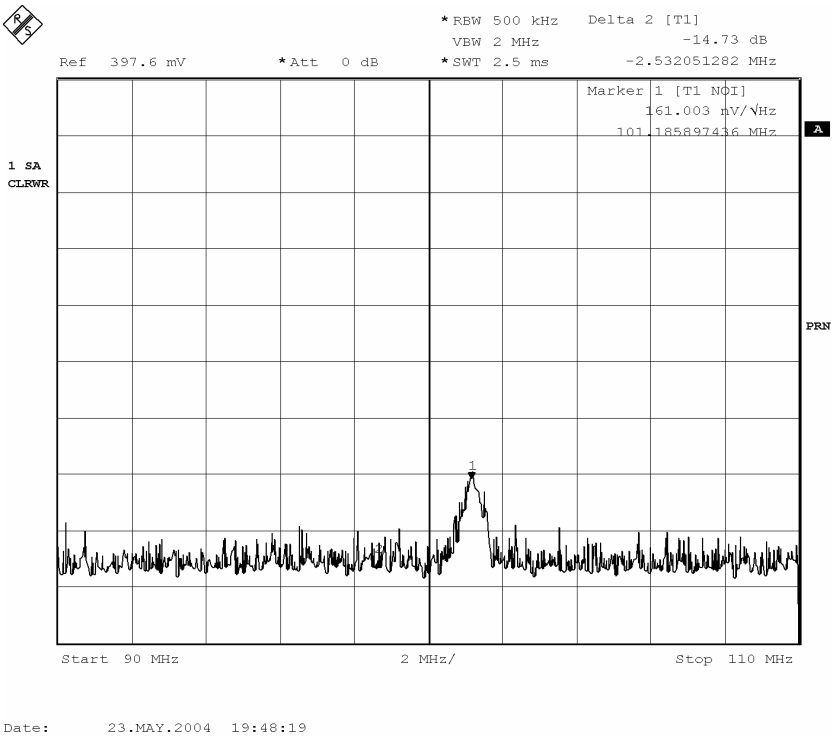


Figure 4.39 Measured Output Noise

Measured output noise is shown in Figure 4.39. The output noise density at 100MHz is $161.0\,nv/\sqrt{Hz}$. Notice from the measured AC response, the voltage gain at 100MHz is 30.6dB. We can calculate the equivalent input noise of the filter circuit as:

$$\tilde{V}_{in,noise} = [161.0 - 4.84]/10^{\frac{30.6}{20}} = 4.69nV/\sqrt{Hz}$$

The measured noise is smaller compared to simulation results. There are several reasons for this: first, the noise models used in simulations might not be accurate; second, and the most likely reason, is that the worst case loss scenarios doesn't happen in chip fabrication. When doing simulations, losses of the internal passive network are estimated for the worst cases considering parasitic capacitance, contact resistances, metal wire resistances, etc. A large gain in the positive feedback path is required to compensate for

all of the losses. However, output noise of a cascode current mirror is proportional to square of the current gain (appendix I). When the actual loss of the internal passive network is smaller than predicted, gain of the positive feedback necessary to boost up Q can be a smaller value, thus dramatically reducing the output noise of current amplifiers.

4.7.4 Measurement of the 1-dB Compression Point

Linearity of the 100MHz filter circuit is evaluated by measurement of 1-dB compression point. 100MHz sinusoid signals are generated from signal generator and fed into the test circuit. Amplitude of the 100MHz tone is varied from -70dBm to -20dBm at a step size of 2dBm. The amplitude of output sinusoid waves is measured using FS8 spectrum analyzer, which is configured for spectrum measurement.

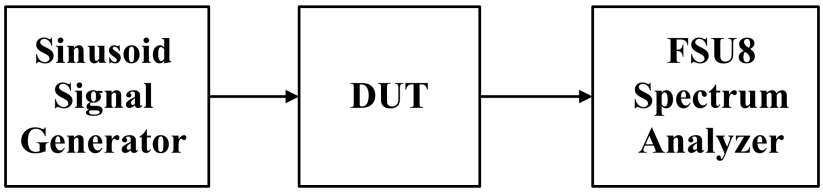


Figure 4.40 Linearity measurement setup

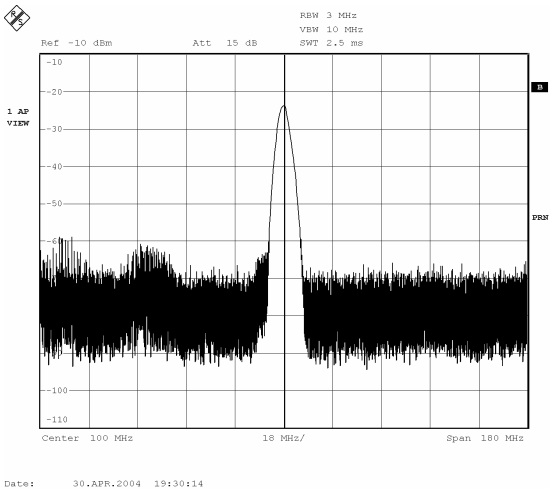


Figure 4.41 Measurement of output spectrum when 100MHz sinusoid is applied to the input

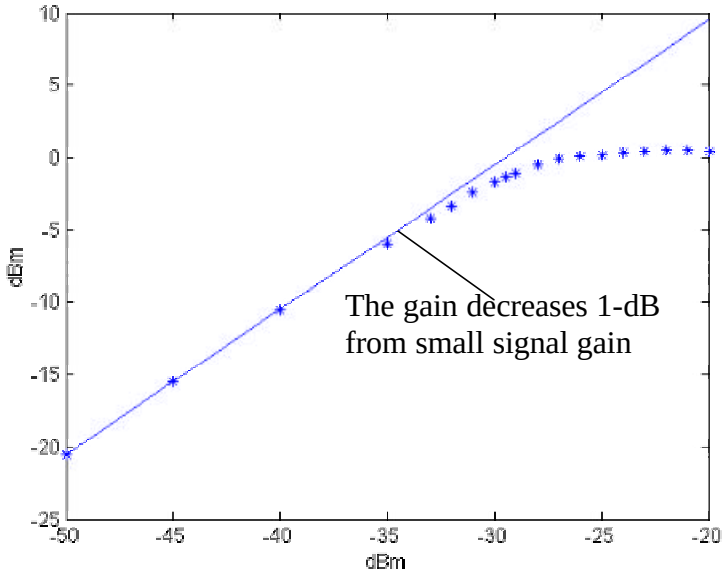


Figure 4.42 1-dB compression point

4.8 Summary

In this chapter, a 100MHz low noise and high Q filter for a FM radio front-end is presented. A summary of experiment and simulation results is listed in Table 4.4. The results verify the theoretical analysis, and proved the feasibility of the novel filter design approach of using current feedback to enhance the Q values of RF filters.

Table 4.4 Summary of Performance

	Simulation Results	Experiment Results
f_0 (MHz)	88 to 108	80 to 110
Q	0.5 to 35	0.5 to 28.9
Equivalent Input Noise @ 100MHz ($nv/\sqrt{Hz}$)	5.68	4.69
1-dB compression point (dBm)	-36.5	-34.0
Dynamic Range (dB)	48.3	54.1
Total DC current (mA)	12	
Chip area (mm^2)	0.5	

CHAPTER 5

A 2.4GHz RF LOW-NOISE HIGH-Q BANDPASS FILTER IN DIGITAL CMOS PROCESSES

Bandpass filters operating at 2.4~2.5GHz frequency band are widely used in Bluetooth and WLAN transceivers for RF band selection and image attenuations. To date, only SAW filters and dielectric filters provide desired performance for these applications. As mentioned previously in this work, an active integrated solution to bandpass filtering at this frequency band has been unattractive due to lack of high quality inductors, high linearity varactors, and low-noise power-efficient active circuitry to compensate for inductor loss and process variations. The situation becomes even worse for wireless applications when power consumption must be minimized to allow for compact size batteries and transceiver sets.

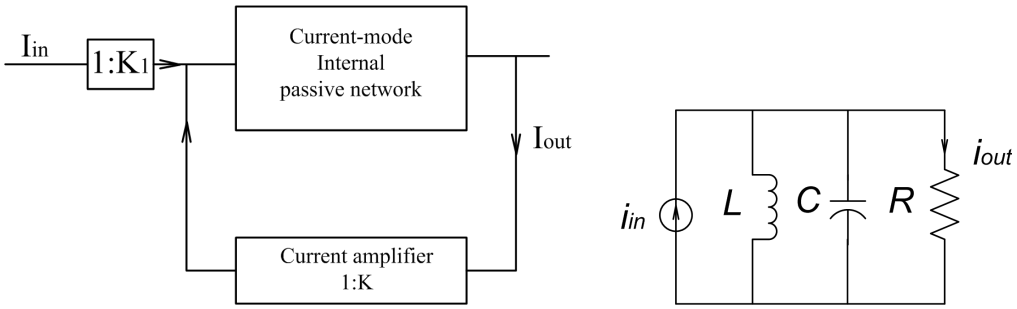
In this work, a 2.4GHz high Q bandpass filter is presented. A current-feedback approach is applied to compensate for parasitic loss through integrated passive elements. Compared to a Q-enhanced LC filter designed based on cross-coupled negative resistance,

we can prove that, to achieve the same Q value, the required amount of DC current is reduced by K times in this work, where K is the current gain of feedback amplifiers. For a typical CMOS process, *K* varies from 3 to 10. The center frequency of the filter is tuned from 2.4GHz to 2.5GHz by varactors, bandwidth of the filter can be varied from 50MHz to 100MHz. The midband gain of the filter can be up to 20dB.

5.1 System Diagram

In Chapter 4, a 100MHz RF low-noise high-Q filter was presented. The filter is designed based on an internal passive RC network and current feedback approach. From the analysis in 4.3.1, we conclude that the core part of the 100MHz circuits, the current amplifiers in the positive feedback path, are suitable for UHF applications due to absence of high impedance circuit nodes. Simulation results showed that the 3-dB bandwidth of a wide-swing cascode current amplifier can be up to 10GHz.

The same topology architecture as discussed in Chapter 4 has been applied to build a 2.4GHz low-noise bandpass and high-Q filter. A lossy LC tank is designed to replace the RC passive internal network for the 100MHz filter. The block diagram of the system is shown in Figure 5.1(a), which is the same as shown in Figure 4.6(a). The lossy LC tank is shown Figure 5.1(b).



(a) System diagram (b) A lossy LC tank

Figure5.1 System architecture

For ease of discussion, at this time we assume all passive elements in Figure 5.1(b) are ideal. The transfer function of the internal passive network, the LC tank, can be expressed as:

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{s\frac{1}{RC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \tag{5.1}$$

Characteristic parameters of the internal RLC network can be extracted from (5.1).

$$\omega_{IPN} = \frac{1}{\sqrt{LC}},\ Q_{IPN} = R\sqrt{\frac{C}{L}}\ ,\ A_{passband\_IPN} = 1 \tag{5.2}$$

Characteristic parameters can be extracted from frequency response of the overall filter, where K is gain of the current amplifier in the feedback path.

$$\omega_0 = \omega_{IPN} = \frac{1}{\sqrt{LC}}$$

$$Q = \frac{Q_{IPN}}{1 - K \cdot A_{passband\_IPN}} = \frac{R\sqrt{\frac{C}{L}}}{1-K} \tag{5.3}$$

$$A_{mid\_band} = \frac{K_1}{1-K}$$

From (5.3), the center frequency of the filter is determined by the resonant frequency of the LC tank. The Q of the filter is determined by the gain in the positive feedback path. A K approaches 1, high Q values are achieved.

There are several advantages of implementing a 2.4GHz RF filter based on the topology shown in Figure 5.1. The first one is the ability to realize high Q. As the value of K is close to 1, the Q factor is boosted avoiding the use of power hungry cross-coupled differential pair negative impedance. The second advantage of this topology is better controllability of Q. To achieve a high Q value, we only need to control the gain of positive feedback path to be less than but close to 1. Consider that the current-mode approach is taken. Also assume the gain of current amplifiers is determined by aspect ratios of mirror transistors, and accurate K values can be obtained with careful arrangement in layout. Only a small amount of power and silicon area is required to build a current amplifier with gain less than 1.

The system shown in Figure 5.1 has the potential to achieve large Dynamic Range (DR). As DR is defined as the difference between the amplitude of the largest input signal which the system amplifies with limited amount of harmonic distortions, and the noise floor, DR is improved by reduced system noise and improved linearity. As with other high frequency LNA designs, noise performance of this system can be optimized by perfect matching to source impedance, and also by increasing the g_m of the input stage. Linearity of the system is improved by the current amplifiers.

Shown in Figure 5.1(b) is a lossy LC tank with ideal inductor and capacitors. However, all integrated passive elements on silicon exhibit losses and parasitic capacitance cannot be ignored in radio frequency designs. Figure 5.2 shows a practical

model of the RLC network shown in Figure 5.1(b). Inductor and capacitor losses are modeled by series resistors, R_L and R_C, respectively.

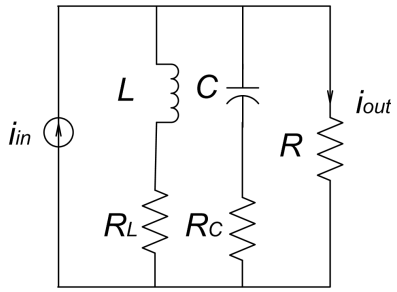


Figure 5.2 modeling the resistive loss of integrated inductors and capacitors

Assume R_L <<R, and R_C<<R, transfer function of the circuit shown in Figure 5.2 can be expressed as:

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{s\dfrac{1}{RC}}{s^2 + s\dfrac{L + CR_CR_L + CRR_L + CRR_C}{LC(R+R_C)} + \dfrac{R+R_L}{LC(R+R_C)}} \tag{5.4}$$

To be consistent with above discussions, w_{IPN} , Q_{IPN} , $A_{passband\_IPN}$ are used to represent the resonant frequency, Q factor and mid-band gain of the circuit in Figure 5.2.

$$w_{IPN} = \frac{\sqrt{R+R_L}}{\sqrt{LC(R+R_C)}} \approx \frac{1}{\sqrt{LC}}$$

$$Q_{IPN} = \frac{(R+R_C)\sqrt{LC}}{L + RC(R_L+R_C) + CR_LR_C} \approx \frac{R\sqrt{LC}}{L + RC(R_L+R_C)} \tag{5.5}$$

$$A_{passband\_IPN} = \frac{\dfrac{1}{RC}}{\dfrac{L + CR_CR_L + CRR_L + CRR_C}{LC(R+R_C)}} \approx \frac{\dfrac{1}{RC}}{\dfrac{1}{RC} + \dfrac{R_L}{L} + \dfrac{R_C}{L}}$$

An example is given below to illustrate the effects of R_L and R_C on performance of the lossy LC tank. Assume *L=2nH*, *C=2pF*, the resonant frequency is then $f_0 = \frac{1}{2p\sqrt{LC}} \approx 2.5GHz$. Assume $R = 100\Omega$, $R_L = 5\Omega$, $R_C = 5\Omega$, the Q factor of the inductor can be calculated as: $Q_L = \frac{wL}{R_L} = \frac{2p \cdot 2.5GHz \cdot 2nH}{5} = 6.28$. In a typical digital CMOS process, the Q factor of inductors is limited by a lot of factors, including process parameters (thickness of metals, metal sheet resistance, capacitance to substrate, etc), geometry parameter (diameter, wire width, shape, etc) and available silicon resources (chip area). Details of inductor designs will be addressed later in this work. Inductors with Q_L ranges from 2~8 are generally achievable by careful arrangement in layout. Based on above assumptions, performance parameters of circuits in both Figure 5.1(b) and Figure 5.2 are calculated, and results are listed in table 5.1.

Table 5.1 comparison of circuits shown in Figure 5.1(b) and Figure 5.2

	Circuit shown in Figure 5.1(b)	Circuit shown in Figure 5.2
Resonant frequency (GHz)	2.5	2.5
Q	3.16	1.58
Mid-band gain	1	0.33

A few observations are made based on results shown in table 5.1. First, the resistive loss of inductor and capacitor dramatic reduces both Q and the gain of the internal passive network. Recall from equation (5.3), Q of the overall system is enhanced if the product of K, gain of positive feedback, and $A_{passband\_IPN}$, mid-band gain of the internal passive network, is close to 1. As $A_{passband\_IPN}$ is reduced due to the existence of

R_L and R_C, a larger value of K is required to obtain the desired amount of Q enhancement. Generally larger area and more power are required to build a current amplifier with large gain, since gain of a current amplifier is basically determined by aspect ratios of mirror transistors. Also, if larger gain stages exist in a system, dynamic range of the system is generally reduced. To minimize the effect of R_L and R_C, high Q inductors and varactors are desirable. This statement is commonly accepted in all RF filter and VCO designs based on LC tanks. [45-49]

5.2 Schematic Circuits

Shown in Figure 5.3 is a simplified schematic. It illustrates how input voltage signals are converted into current signals, how the internal passive network is built and how the positive feedback is formed. Practical design issues such as the input impedance matching, gain control of current amplifiers, details in bias circuitry, and common-mode feedback, are to be addressed later in this chapter.

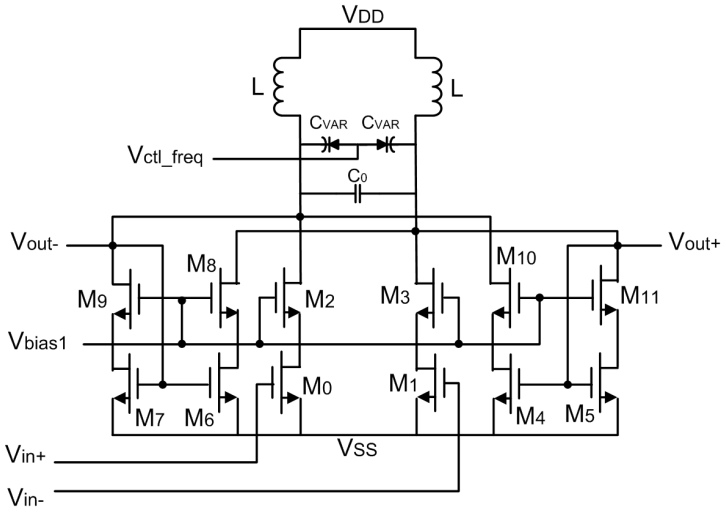


Figure 5.3 A simplified schematic of 2.4GHz RF front-end filter and amplifier

As shown in Figure 5.3, transistors M_0 and M_1 form the input stage, which transforms input voltage signals into current signals. The design objective of the input stage is twofold. First, since the input stage interfaces with source or a stage precedes the RF filter/amplifier, the input impedance looking into the input stage should match that of the source or output impedance of the preceded stage. Second, the noise performance of the overall system depends heavily on the effective transconductance of the input stage. Therefore, the effective transconductance of the input stage is to be maximized to optimize noise performance of the overall system.

Shown in the middle of Figure 5.3 are inductors, fixed capacitors and varactors. These passive elements, together with the resistance looking into drain of M_9 and M_{11}, form the internal 'passive' network. Guidelines for determining values of passive components are given below:

- Resonant frequency of the system is determined by the product of L and C
- Gain of the internal passive network is to be maximized to potentially reduce power consumption and facilitate the gain control of current amplifiers. According to equation (5.5)

$$\max\left\{A_{passband\_IPN}\right\}_{LC=\frac{1}{(2pf)^2}} = \max\left\{\frac{\frac{1}{RC}}{\frac{1}{RC}+\frac{R_L}{L}+\frac{R_C}{L}}\right\}_{LC=\frac{1}{(2pf)^2}} \qquad (5.6)$$

$$= \max\left\{\frac{1}{1+(2pf)^2 RC^2(R_C+R_L)}\right\}$$

To maximize the gain of the internal passive network, the second term in the denominator of equation (5.6) should be minimized. As a result, smaller values of R_L and R_C are desirable. If R_L and R_C are zero, maximum value of mid-band gain,

1, is achieved, which verifies the results derived from the circuit shown in Figure 5.1(b). Also, to maximize the mid-band gain, small values of R and C are desired.

- Capacitance value, C should be small to make mid-band gain of the internal passive network as large as possible; on the other hand, C should be large enough such that effect of parasitic capacitance associated with other circuit components can be 'absorbed'.
- Two groups of capacitors are designed, C_{FIXED} and C_{VAR}. Fixed capacitance, C_{FIXED}, is realized by poly-poly capacitors to optimize linearity performance; Variable capacitance, C_{VAR}, is implemented by accumulation mode MOS varactors to tune the resonant frequency at the presence of process and environment variations.

In Figure 5.3, transistors M_6, M_7, M_8 and M_9 form a positive feedback path, and transistors M_4, M_5, M_{10} and M_{11} form a same feedback path for differential operations. Gain control of the current amplifier is omitted in Figure 5.3. Details on gain control will be described later in this chapter.

5.2.1 Input Impedance Matching

Since the circuit is designed differentially, transformer baluns are required for the circuit to interface with single-ended test equipment. When off-chip baluns are used, input impedance matching circuit is shown in Figure 5.4.

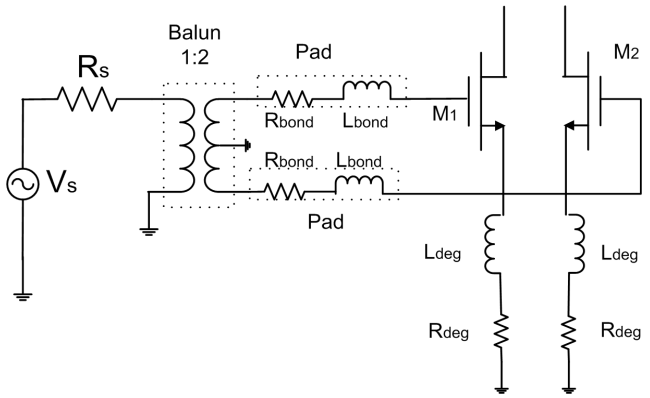


Figure 5.4 input impedance matching circuitry

When the design is packaged for testing, bondwire inductance and resistance are resulted from packaging process. Let L_{bond} and R_{bond} denote bondwire inductance and resistance resulted from connections to bonding pads, respectively. A degeneration inductor, L_{deg}, is placed at the source of M_1, the series resistance associated with L_{deg} is represented by R_{deg}. To calculate the impedance seen from the input terminal, a small-signal equivalent circuit of Figure 5.4 is shown below in Figure 5.5.

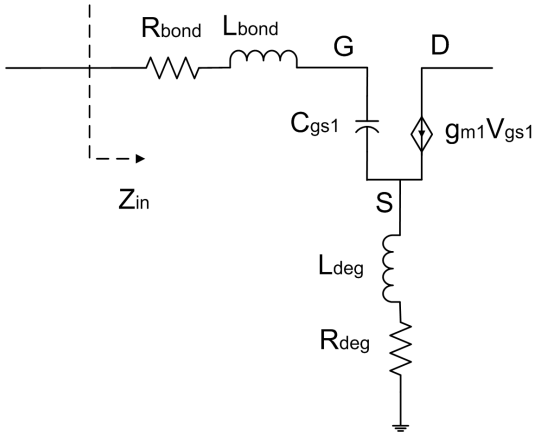


Figure 5.5 small-signal equivalent circuit of the input stage

From Figure 5.5, we can derive the expression for the input impedance:

$$Z_{in} = R_{bond} + R_{\deg} + g_m \frac{L_{\deg}}{C_{gs}} + j\omega(L_{bond} + L_{\deg}) + \frac{g_m R_{\deg}}{j\omega C_{gs}} \tag{5.7}$$

To make the input impedance of the circuit match the source resistance,

$$Z_{in} = R_s$$

$$\rightarrow R_{bond} + R_{\deg} + g_m \frac{L_{\deg}}{C_{gs}} = R_s \tag{5.8}$$

$$j\omega_0(L_{bond} + L_{\deg}) + \frac{g_m R_{\deg}}{j\omega_0 C_{gs}} = 0$$

Assume g_m=20mS, C_{gs}=4pF, L_{bond}=1.2nH, $R_{\deg} = 2\Omega$, solve equations in (5.8) yields:

$$L_{\deg} = 0.9nH$$

$$R_{\deg} = 43\Omega$$

By careful arrangement in layout, spiral inductors can be designed to achieve both inductance value and series resistance simultaneously, avoiding the need for additional resistors.

Another version of the test circuit is designed with an on-chip transformer balun. The input matching circuitry is very similar to Figure 5.4 except that balun and bonding pad swap their positions. Design of on-chip baluns will be discussed in details later in this chapter.

5.2.2 Design of the Variable Gain Current Amplifier

As mentioned earlier, the gain of current amplifiers in feedback path is varied to tune the Q of the filter. The schematic of the variable gain current amplifier is shown below in Figure 5.6. Design parameters are listed in table 5.2. When binary control signals are applied to switches S0~S5, gain of the current amplifier varies from 1.5 to 5.5, at a resolution of 0.0625. In other words, there are 64 steps of increments from 1.5 to 5.5, with a step size of 0.0625. The gain will be one of the 64 discrete values. Small step size is chosen since Q of the overall system is sensitive to the gain of current amplifier especially as Q value is large.

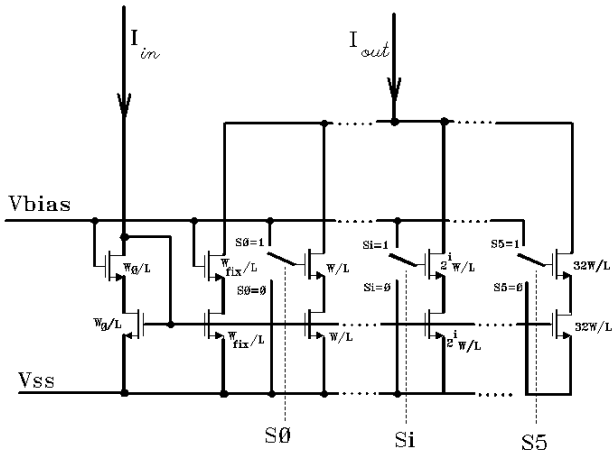


Figure 5.6 schematic of the variable gain current amplifier

Table 5.2 Design parameters of variable gain current amplifiers

S5	S4	S3	S2	S1	S0	Bias current	Current gain
0	0	0	0	0	0	0.8mA	1.5
0	0	0	0	0	1	0.8375mA	1.5625
0	0	0	0	1	0	0.875mA	1.625
0	0	0	1	0	0	0.95mA	1.75
0	0	1	0	0	0	1.1mA	2.0
0	1	0	0	0	0	1.4mA	2.5
1	0	0	0	0	0	2mA	4.5

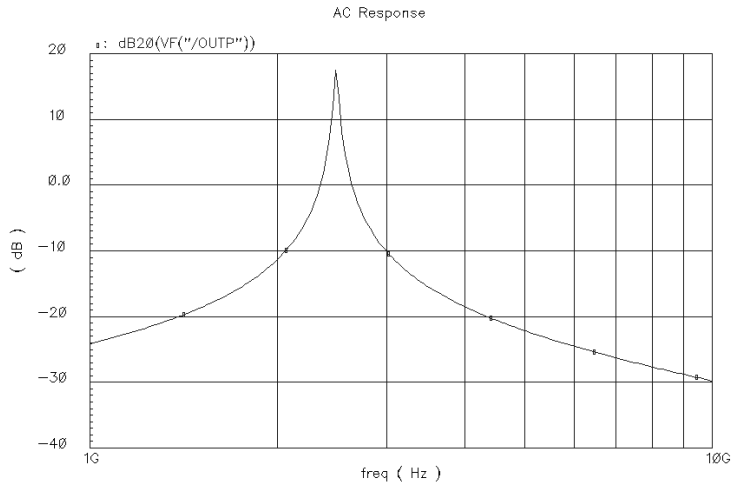
5.3 Simulation Results

5.3.1 AC Responses

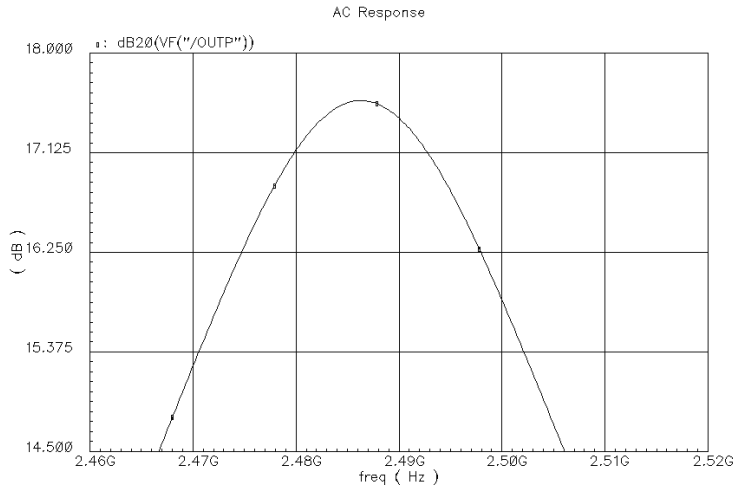
A typical AC response is shown in Figure 5.7(a). Plot of the AC response at the vicinity of center frequency is shown in Figure 5.7(b). Simulation results showed that the center frequency can be tuned from 2.4GHz to 2.5GHz, also bandwidth is tunable from 25MHz to 200MHz.

For the AC response shown in Figure 5.7(b), Q of the filter can be calculated as:

$$Q = \frac{center\_frequency}{3-dB\_bandwidth} = \frac{2.487GHz}{2.505GHz - 2.468GHz} = 67.2$$



(a)



(b)

Figure 5.7 Frequency response

5.3.2 Noise

There are several ways to characterize the noise performance of RF circuits including input noise spectrum density, output noise spectrum density and noise figure. In this work, equivalent input noise spectrum density is used to characterize the noise performance. A

plot of the equivalent input noise is shown in Figure 5.8. The noise spectrum density at 2.4GHz is $2.39\,nV/\sqrt{Hz}$ ..

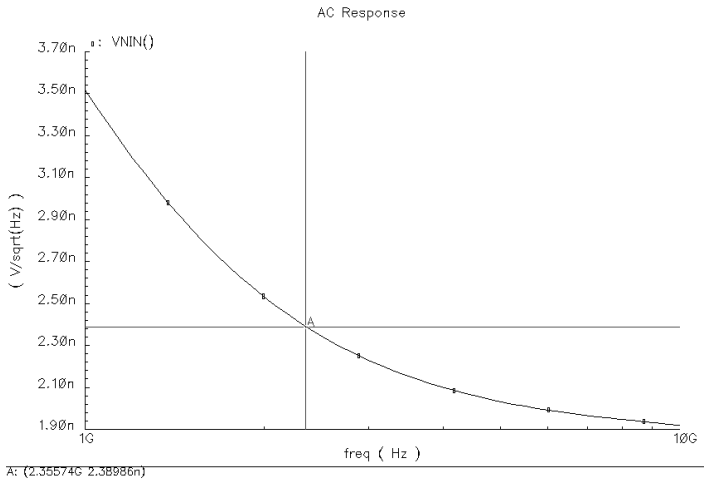
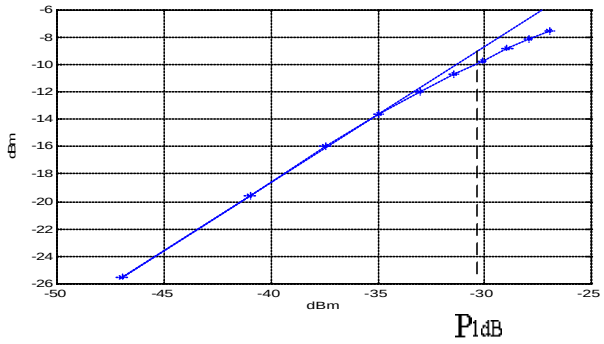


Figure 5.8 Equivalent input noise

5.3.3 Linearity

5.3.3.1 1-dB Compression Point

Linearity of the circuit is evaluated using the 1 dB compression point. A plot of output power vs. input power is shown in Figure 5.9. The 1-dB compression point is the input point where the circuit gain decreases 1 dB from the small signal gain, which is -30.7dB as shown in Figure 5.9.


-6
-8
-10
-12
-14
-16
-18
-20
-22
-24
-26
dBm
-50
-45
-40
-35
-30
-25
dBm
P1dB

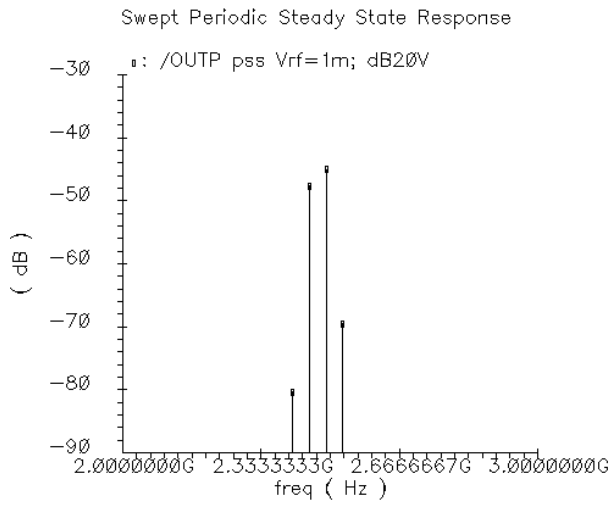
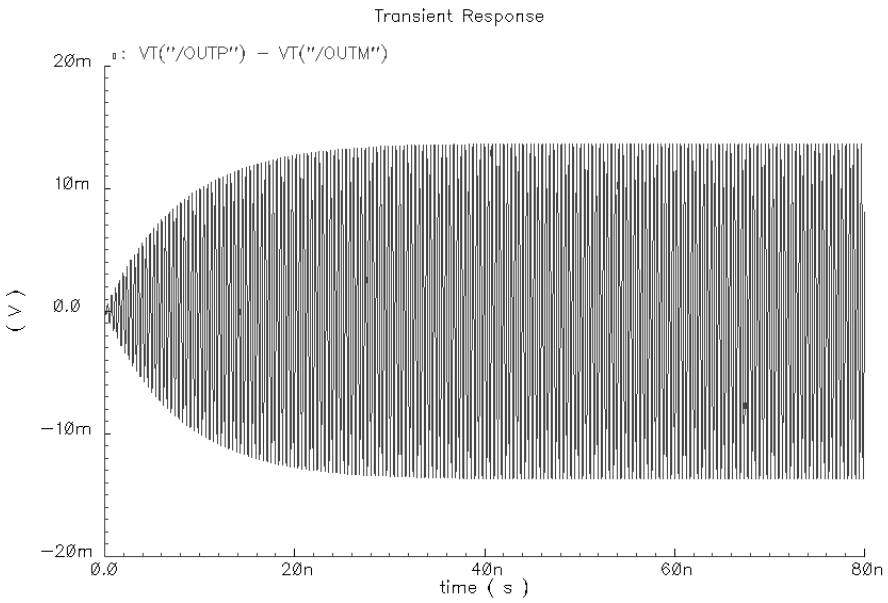


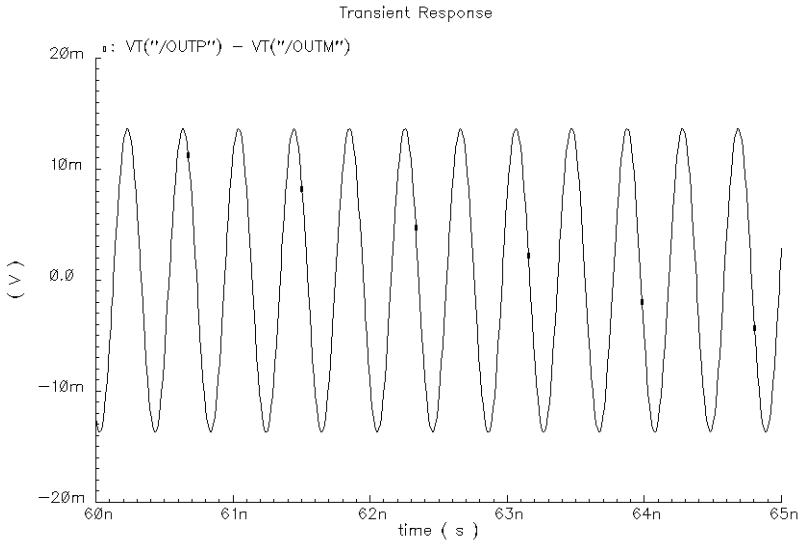
Figure 5.10 The two-tone test result

5.3.4 Transient Analysis

Transient analysis is performed to verify the stability of the circuit. As shown in Figure 5.11(a), the system is stable and reaches steady state in around 20 ns after a 1mV sinusoid signal is applied to the input terminals. Steady state transient response is shown in Figure 5.11(b). Observe that there are no distortions around peaks and no slew occurs when output voltage changes between negative peak values to positive peak values.



(a)



(b)

Figure 5.11 Transient analysis simulation results (a) The transient response within time interval [0 80ns] (b) The transient response within time interval [60nS 65nS]

5.4 Layout and Implementation

5.4.1 Design of On-chip Inductors

On-chip inductors, especially the inductor in LC tank, are key elements of successful implementation of this design. Perfect round wires are preferable to maximize Q value of on-chip inductors. However, it may not be practical to build such wires in some CMOS processes. In the process that this design is fabricated, only horizontal, vertical or 45 degree oriented wires are allowed. As a result, octagonal wires are the best approximation of round wires. Top metal layers (metal 6 and metal 5) are generally preferred for high performance tank inductor because they are usually thicker and have low parasitic capacitance to substrate.

Design parameters of the tank inductors are listed in Table 5.3.

Table 5.3 Design parameters of tank inductor

	Version 1
Metal layer	5
Transition metal layer	4
Metal sheet resistance (min/typ/max) milliohm	32/36/40
Metal thickness (min/typ/max) nm	809.5/859.5/909.5
Shape	Octagon
Radius (um)	160
Wire Width (um)	15
Number of turns	2
Wire to wire separation (um)	2
Space for transition	20
Inductance (nH)	2.08
Series resistance (ohm)	7.86
Rsub1	2.11
Rsub2	0.23
Csub1 (fF)	114
Csub2 (fF)	116
Q @ 2.4GHz	3.8
Self resonant frequency (GHz)	10.3

A patterned ground shield is placed in the N-well to decrease eddy current loss through substrate. It's been reported that grounded metal slices on metal 1 or poly silicon can effectively reduce substrate loss [64]. However, inserting the patterned ground shield on metal 1 or poly layer increases parasitic capacitance from the tank inductors to ground. Building patterned ground shield in N-well has been verified to be the optimal way to reduce substrate loss and enhance Q value of inductors [65].

In this work, patterned ground shield is build using N-well slices. The width of each N-well slice is 4um, and the orientation of each N-well slice is orthogonal to that of the inductor segments it intersects, such that current flow in ground shield is orthogonal to that of the signal current flow through inductors. Ends of N-well slices are connected to allow ground current to flow in the way described above. All N-well slices are connected to Vdd, which is AC ground. Tank inductor designed on metal 5 is shown in Figure 5.12.

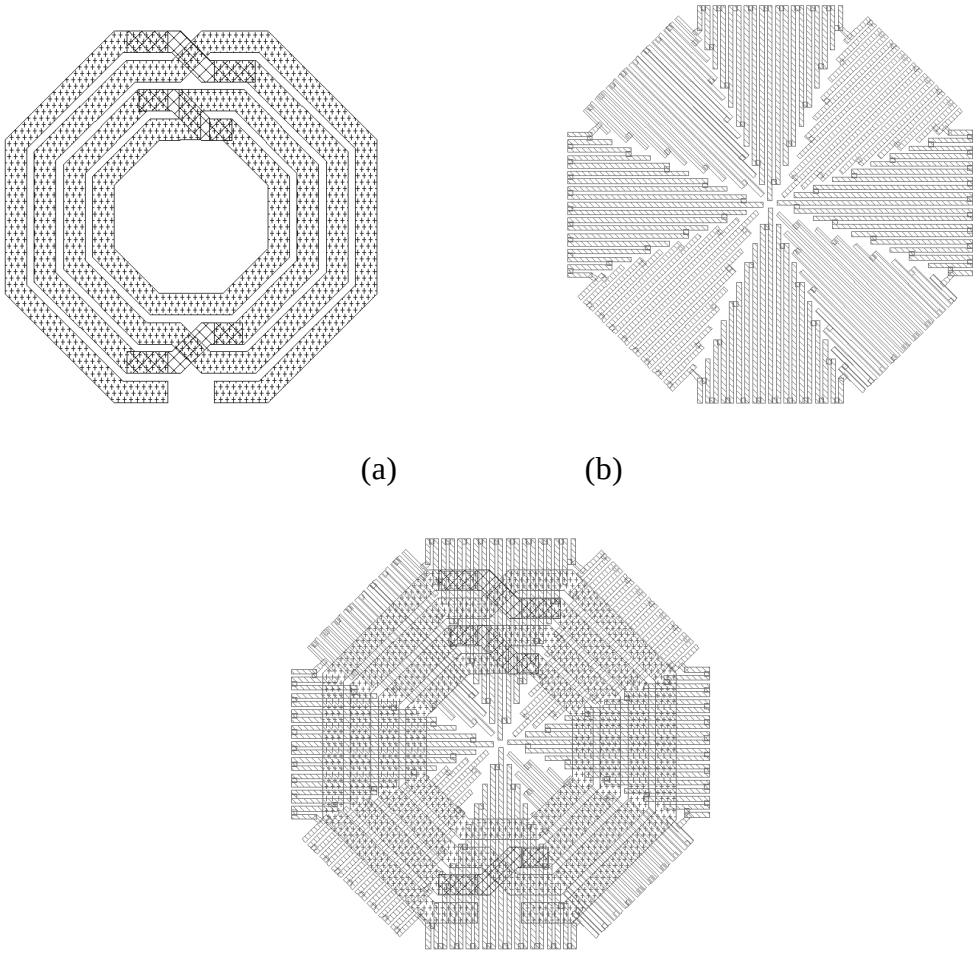


Figure 5.12 (a) top metal octagonal inductor (b) patterned ground shield in Nwell (c) topview of tank inductor

As mentioned earlier, degeneration inductors are required in the input stage such that the input impedance matches that of the source. Source degeneration inductors are designed in similar ways as for tank inductors, except that requirement on Q can be relaxed due to large resistance values. Calculations showed that large series resistances (~40ohms) are associated with the inductors (~1nH), therefore low-Q inductors are

sufficiently suitable. Compared to high-Q tank inductors, degeneration inductors have narrower wire width, smaller area, and can be less accurate.

5.4.2 Design of Varactors

Frequency tuning of this design is implemented by varactors. The total load capacitance includes two parts, fixed and variable capacitance.

$$C_{load} = C_{fixed} + C_{VAR}$$

To determine the range of capacitance values that the varactors need to realize, we need to consider both the desired tuning range of the center frequency and process variations during fabrication. Since the center frequency of the system is the same as the resonant frequency of load LC tank, $w_0 = \frac{1}{\sqrt{LC_{load}}}$, a 20% change in frequency requires 40% change in total load capacitance. Poly-poly capacitors experience 20% variations in capacitance values during manufacture process. C_{VAR} varies from 0.2pF to 1.2pF to compensate for process variations and achieve the desired frequency tuning.

The accumulation mode MOS varactors are built by placing heavily doped n+ regions in N-Well. A structure for the varactor is shown below in Figure 5.13.

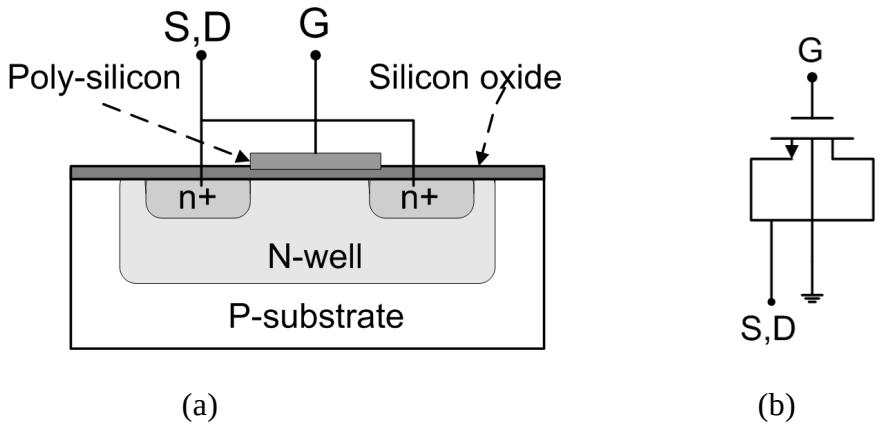


Figure 5.13 (a) accumulation mode MOS varactor (b) symbol

Layout of the MOS varactors is shown in Figure 5.14. Multiple finger NMOS devices are designed to reduce series resistance thus increase Q value of varactors. Size of NMOS transistors are 8(8um/2um). Simulation results of capacitance values vs. the gate-source voltages are shown in Figure 5.15.

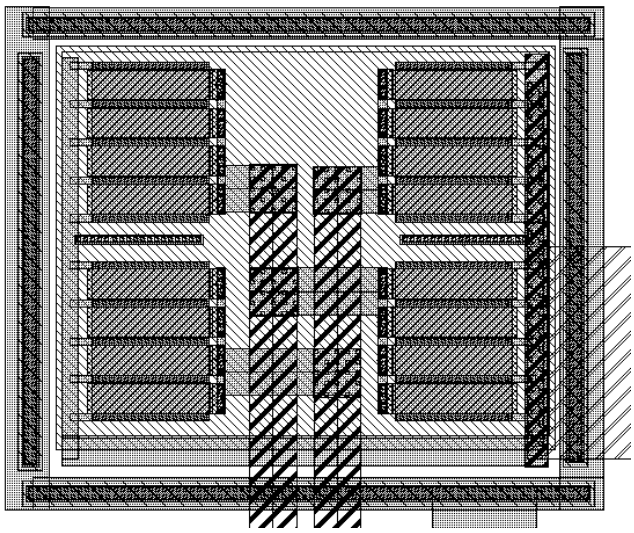


Figure 5.14 Layout of accumulation mode MOS varactors

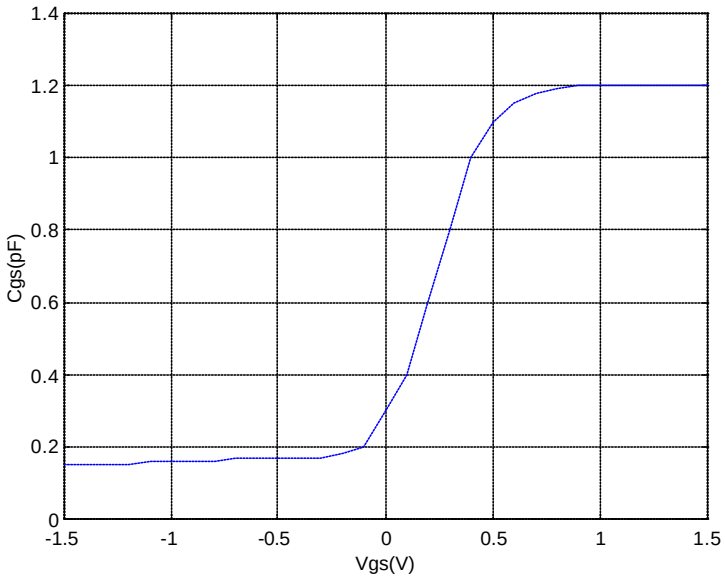
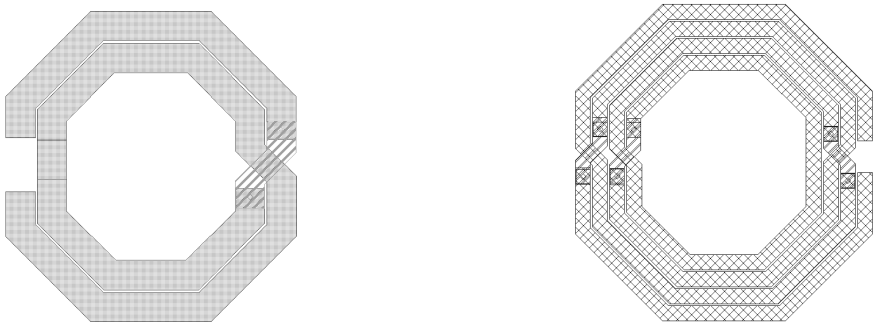


Figure 5.15 Capacitance values vs. control voltage

5.4.3 Design of On-chip Baluns

To interface with single-ended measurement equipment, on-chip transformer baluns are designed (Figure 5.16). Design parameters of these transformer baluns are listed in Table 5.4.



(a) (b)

Figure 5.16 (a) Primary coil, (b) Secondary coil

Table 5.4 Integrated baluns -- Design Parameters

	Primary coil	Secondary Coil
Metal layer	1	5
Transition metal layer	2	2
Shape	Octagon	Octagon
Radius	150	150
Wire width (um)	30	15
Number of turns	2	4

The input impedance matching circuit is slightly different as shown in Figure 5.17 due to integration of transformer baluns (Figure 5.15).

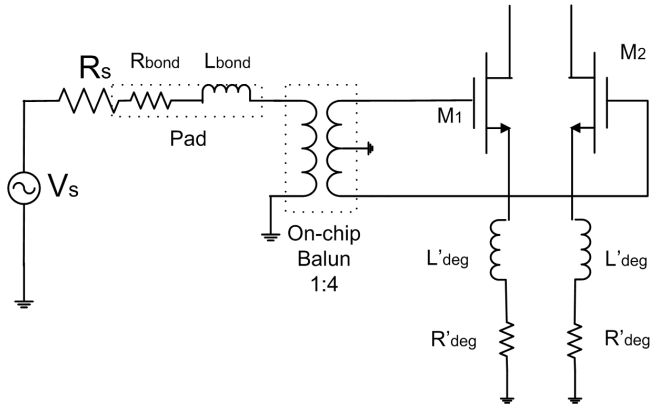


Figure 5.17 The input impedance matching circuit with on-chip transformer balun

5.4.4 Layout

A complete layout of the 2.4GHz filter is shown in Figure 5.18. On the right of the layout are two test baluns, which are not connected to the rest of the circuit. Separate baluns allow measuring and subtracting the effect from the overall system responses. The center part of the layout is the input balun, which converts single-ended input signals into differential signals. The left part of the layout is the main circuitry. We can tell that there are three inductors shown in this part: On the top is the tank inductor, and at the bottom are the two inductors which help input impedance matching by source degeneration. Also in the main circuitry are input transistor arrays, variable gain current amplifiers, poly-poly capacitor arrays, varactors, switch control logic circuitry and buffers.

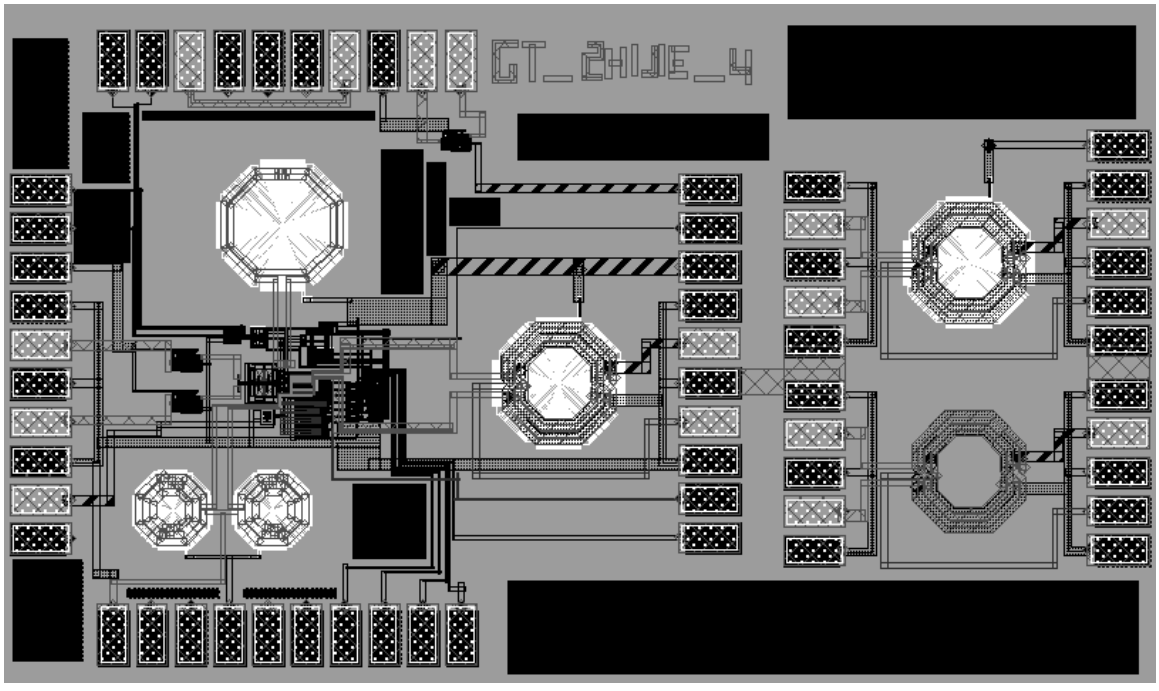


Figure 5.18 Layout of 2.4GHz filter

The circuit was sent to the NSC 0.18 um CMOS process for fabrication, and is to be packaged using Thin Shrink Small Outline Packaging TSSOP56. Due to the delay in the packaging process, the parts are to be tested after this thesis is done and the experiment results are to be published upon finishing.

CHAPTER 6

CONCLUSIONS

6.1 Summary of This Work

This work focuses on the design of RF low-noise and high-Q bandpass filters and amplifiers in standard digital CMOS processes. Two circuits are designed in this thesis: a 100MHz low-noise and high Q bandpass filter suited for an FM radio front-end, and a 2.4GHz low-noise and high-Q bandpass filter suited for a Bluetooth front-end.

Current-mode approach and positive feedback design techniques are successfully used in the design of both circuits. Application of current-mode approach helps removing high impedance circuit nodes, and inherently increases operating frequencies; Positive feedback is used to compensate for loss of integrated passive elements and to boost the Q value of integrated filters.

The 100MHz tunable low-noise bandpass filter was fabricated through the NSC 0.18um CMOS process. The silicon area of the core circuit is $0.4 mm^2$. The circuit achieves 3.15uV RF sensitivity with 26dB SNR, and the total current consumption is 10mA. The center frequency of the filter is tunable from 80MHz to 110MHz, and the Q value is tunable from 0.5 to 28.9. The 1 dB compression point is measured as -34.0dBm, combined with noise measurement results, gives a dynamic range of 54.1 dB.

The 2.4GHz tunable low-noise bandpass filter is also fabricated through the NSC 0.18um CMOS process. Silicon area of the core circuit is $1\,mm^2$. Integrated spiral inductors are developed for this design. The patterned ground shields are laid out to reduce inductor loss through substrate, especially eddy current loss when the circuit is fabricated on epi wafers. Accumulation mode MOS varactors are designed to tune the frequency response. Based on simulations, the system achieves a 4.6dB noise figure. The center frequency of the circuit is tunable from 2.4GHz to 2.5GHz, and the Q value is tunable from 20 to 120. The 1 dB dynamic range of the circuit is 50dB.

6.2 Contributions

Contributions of this work include:

- A novel design approach: Design of CMOS RF low-noise and high-Q filters using the current feedback approach

This thesis present a novel design technique for building high performance CMOS RF bandpass filters and amplifiers which are intended to replace the off-chip discrete filters currently used in most RF receivers. The performance of the two circuits designed in this thesis makes possible a fully integration of wireless front-ends, especially when the front-end architecture is designed as described in Chapter 4.

In this work, current-mode approach together with positive feedback techniques have proved successful in building ultra high frequency and high performance integrated filters. Current-mode circuits simplify the construction of feedback circuits by removing buffers

and summing circuits which are necessary if the same circuit is implemented using voltage-mode approach.

Systematic analysis is performed to provide insights on critical design issues concerning RF high Q filters while maintaining stable operations. Performance of the circuits is optimized while allowing minimum number of discrete elements.

- Design of a ultra wideband variable gain current amplifier

In this work, a variable gain wide swing cascode current amplifier is designed. Gain of the current amplifier is binarily controlled such that the filter circuits achieve the desired Q tuning range. The variable gain current amplifier offers precise current amplification over a wide bandwidth, which makes it ideal for gigahertz applications. Both the 100MHz circuit and 2.4GHz circuit designed in this work adopt the variable gain current amplifier in the positive feedback path, and it is proved that the amplifier provides satisfactory performance over both frequency ranges (80MHz to 110MHz, and 2.4GHz to 2.5GHz).

- A novel cross-coupled negative resistor

The above mentioned variable gain current amplifier can be used to build a novel cross-coupled CMOS resistor. It is showed that the approach is very successful when building small resistors (large g_m) under power constraint. To achieve the same g_m value, only a fraction of DC currents is required compared to the same resistors built using simple cross-coupled differential pairs.

6.3 Future Work and Discussions

- Design of high order high Q filters

Both circuits designed in this work are second-order bandpass filters/amplifiers (biquads). According to specific transceiver architectures, a single biquad cannot provide enough attenuation for image and interference signals and high order filters need to be developed based on these biquads.

- Performance analysis under temperature variations

The RF circuits designed in this work are intended for use in wireless receivers, which work in an environment with large temperature variations. At extreme temperatures, the design is to guarantee that the variation of center frequency and Q is small enough such that the desired signal channel stays in band all the time. Meanwhile, the design should guarantee the stability of the systems at extreme environment temperatures.

- Substrate modeling – to reduce substrate noise

As stated earlier, any building blocks which stay close to antenna must be low-noise to achieve the desired detection sensitivity and maintain required SNR. Noise performance of both circuits designed in this work is optimized concerning thermal noises generated inherently by transistors and resistors. However, when the circuits are built on the same substrate as noisy digital circuits, substrate coupling becomes a major noise source. Substrate modeling helps us understanding and simulating the effects of substrate noise on the performance of the circuits, and improves the design accordingly.

Appendix A

The Noise of a Wide-swing Cascode Current Amplifier

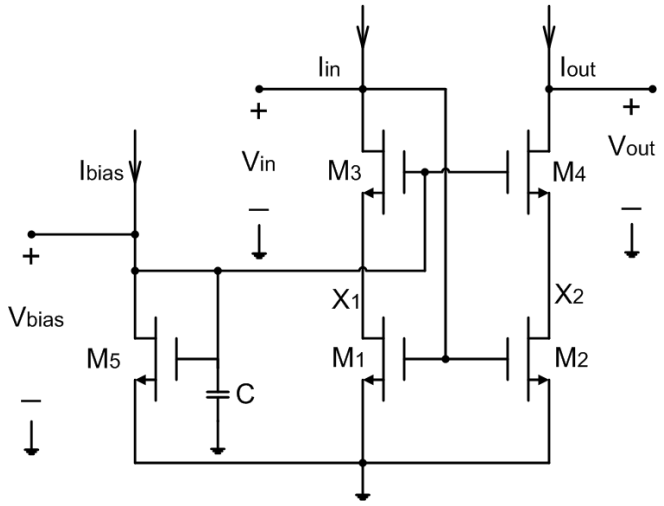


Figure A-1. A new drawing of cascode current mirror for noise analysis

Noise of cascode current mirror in FigureA-1 is mainly determined by noise generated from M1 and M2. M3 and M4 contribute negligibly to the output, especially when capacitive loads at nodes X1 and X2 are small enough around working frequencies. In this analysis, flicker noises are ignored for simplicity.

- Output noise contributed by M2 and M4

Noise output generated by M2 and M4 are evaluated based on Figure A-2.

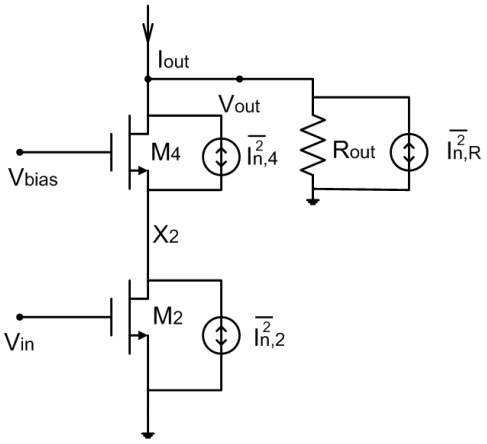


Figure A-2 Output noise generated by M2 and M4

To calculate noise output caused by M2 and M4, the input terminal, Vin , is grounded. Three noise sources are shown in Figure 2. Noise spectrum density functions are:

$$\overline{I_{n,2}^2} = \frac{8}{3} kTg_{m2}$$

$$\overline{I_{n,4}^2} = \frac{8}{3} kTg_{m4}$$

$$\overline{I_{n,R}^2} = 4kT \frac{1}{R_{out}}$$

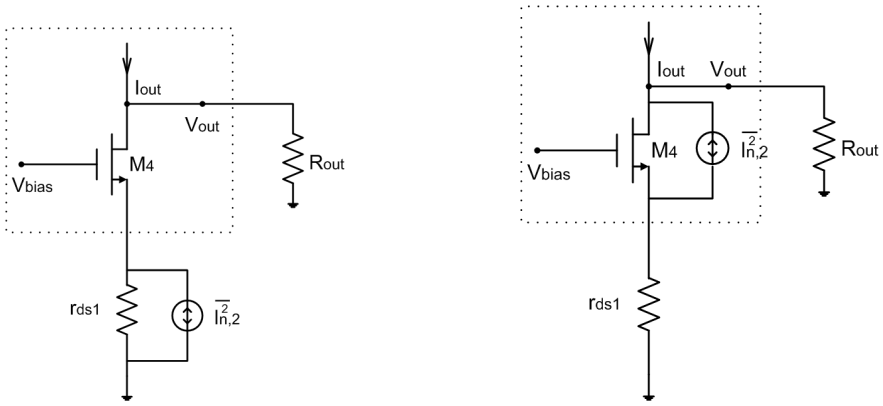
Since noises generated from M2, M4 and Rout are uncorrelated, the total output noise can be obtained by the sum of output noise caused by each of the three noise sources while the other two noise sources generate zero noise.

Illustrated in Figure 3 are equivalent noise models when the input is short to ground. From Figure A-3(a), we can see that the noise current flowing through the load

resistor is the same as the noise current associated with M2. This is simply because the total current flow into the dotted box in Figure A-3(a) is zero to achieve charge balance. Output noise contributed by M2 is expressed as:

$$\overline{V_{n,2}^2} = \frac{8}{3} kTg_{m2} R_{out}^2$$

Contribution of M4 to the total output noise is negligibly small. Ignore channel modulation of M1, and assume the channel resistance rds1 is infinity. Also assume the parasitic capacitance at node X2 in Figure A-1 is small such that frequency of the parasitic pole associated to this node is much higher than frequencies of interest. From Figure A-3(b), we can see that there are no currents flowing out of the dotted box to rds1, therefore the noise current flow to Rout is also zero.



(a) (b)

Figure A-3 Equivalent noise models as the input is short to ground

It is straight forward to see that the output noise generated by the load resistor itself is:

$$\overline{V_{n,R}^2} = 4kTR_{out}$$

The total output noise generated by M2 and M4 can be expressed as:

$$\overline{V_{n,M2,M4,R}^2} = \frac{8}{3}kTg_{m2}R_{out}^2 + 4kTR_{out}$$

- Output noise contributed by M1 and M3

Redraw the circuit in Figure A-4 to find out how M1 and M3 affect the noise performance at the output. Assume M2 and M4 are noiseless, and performing current mirror functions as they normally do.

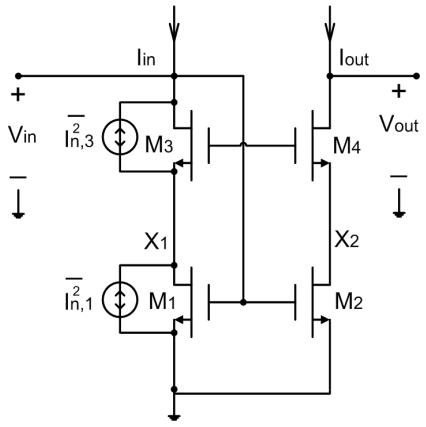


Figure A-4 Noise contributions from M1 and M3

Again, to obtain output noise, the input, Vin, is shorted to ground. In this scenario, it's convenient to represent the total noise of M1 and M3 by an equivalent input noise current source. Similar to the analysis for M4, thermal noise generated by M3 contributes little to the total input noise currents, and the equivalent input noise current is mainly determined by that of M1. Thus:

$$\overline{i_{in,eq}^2} = \frac{8}{3} kTg_{m1}$$

This noise current is mirrored to the output side, and contributes to the total output noise current:

$$\overline{i_{out,M1,M3}^2} = \frac{8}{3} kTg_{m1}\left(\frac{g_{m2}}{g_{m1}}\right)^2 = \frac{8}{3} kTg_{m2}\left(\frac{g_{m2}}{g_{m1}}\right)$$

- Output noise contributed by DC bias circuits

At high frequencies, noise generated by DC bias circuits is shorted to ground by capacitor C. At low frequencies, noise from DC bias circuitry is represented by an equivalent noise voltage source, as shown in Figure A-5.

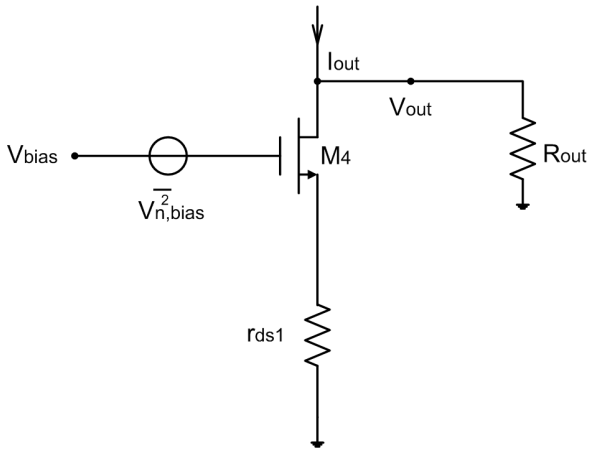


Figure A-5 Noise generated by DC bias circuitry

Transfer function from Vbias to Vout can be expressed as:

$$\frac{V_{out}}{V_{bias}} = \frac{g_{m4} R_{out}}{1 + g_{m4} r_{ds1}}$$

Ignoring the channel modulation of M1 and assuming rds1 is much larger compared to the output resistance, gain from Vbias to Vout is very small, and DC bias circuitry has very little effects on output noise.

- Conclusions
  - Total output noise current of a cascode current mirror is:

$$\overline{i_{out,n}^2} = \frac{8}{3} kTg_{m2}\left(1 + \frac{g_{m2}}{g_{m1}}\right) + 4kT\frac{1}{R_{out}}$$

  - Cascode transistors M3 and M4 don't contribute to output noise
  - DC bias circuitry does not affect noise performance

Appendix B

The Convergence Problems in Simulations of High-Q Bandpass Filters

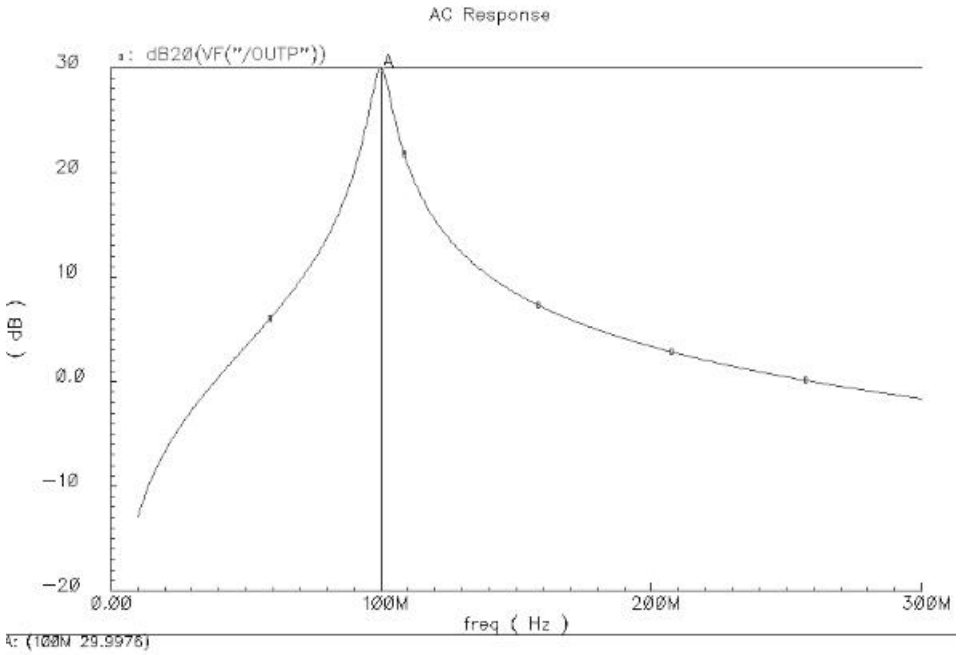
--- Observations in AC Response Simulations

Design of integrated high-Q bandpass filters has been a most challenging topic in IC design industry for the past ten years. It's of essential importance to accurately model and simulate the behavior of a high-Q bandpass filter. However, as Q gets higher, convergence becomes more of a problem due to the existence of high-Q poles and tendency to oscillating, and reliability of simulations results becomes questionable.

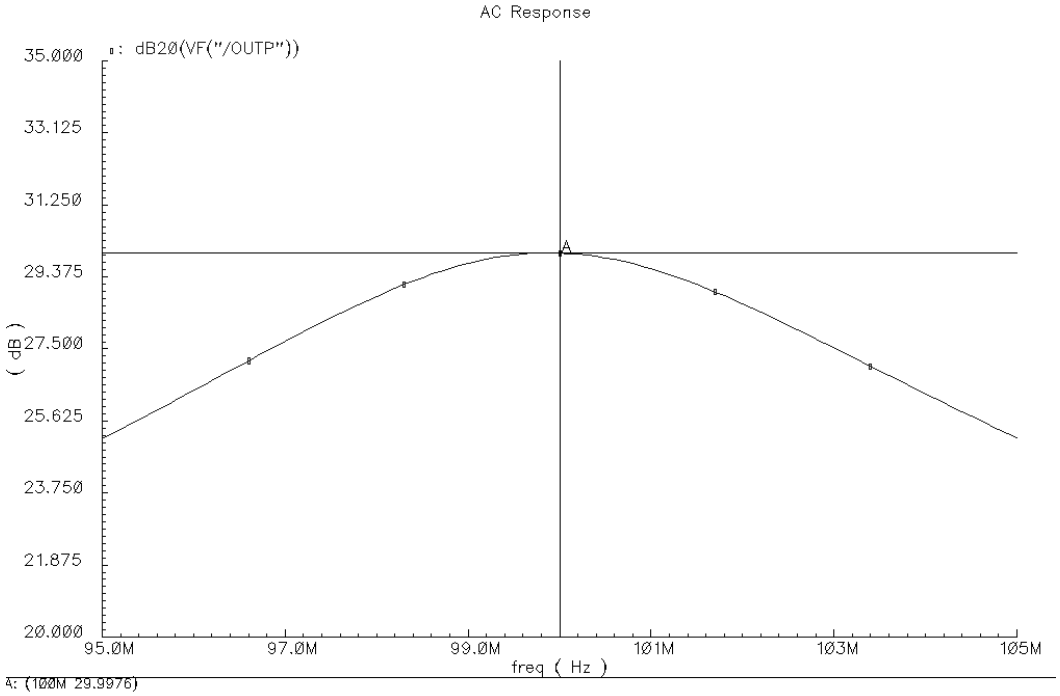
Frequency responses, also called AC responses, or transfer functions, are used to describe behavior of circuits in frequency domain. There are two approaches to obtaining AC responses using simulation software such as Spectre or SPICE. In most cases, the first approach is named 'AC analysis'. AC analysis is a small signal, linear analysis. Circuits are linearized for AC analysis through an operating point calculation. The second approach to AC simulations is to apply a sinusoid signal to the input of the test circuit,

perform ‘Transient analysis’, obtain transient output signals, and calculate gain and phase shift by comparing the output transient signal to the sinusoid input. Repeating above operations while varying the frequency of input sinusoid wave, a group of data points are collected and AC response can be extrapolated from these data points. Theoretically, the two analysis approaches described above should yield same results. However, observations from simulation results of the 100MHz bandpass filter designed in Chapter 4 with Q of 25 showed that different AC responses are obtained using the two simulation approaches. When transient analysis is performed, the magnitude of input signals is chosen as 1mV peak, which is well below the 1 dB compression point and harmonic distortions are negligible.

An AC response obtained using ‘AC analysis’ is shown in Figure B-1. Plotted in Figure B-1(a) is the AC response over the frequency range from 10MHz to 300MHz; Figure B-1(b) is a zoom in version of (a) at around the peak frequency. We can see that the center frequency is 100MHz, and mid-band gain is 30dB.



(a)



(b)

Figure B-1 AC analysis simulation result

The second approach is also used to obtain AC response simulations for the same circuit. When performing this transient analysis, the convergence criteria is set to 'conservative'. The amplitude of input sinusoidal signals is set to the middle of the input dynamic range, such that effects of both noise and distortions are minimized. Figure 2 shows a plot of AC simulation results obtained using this approach.

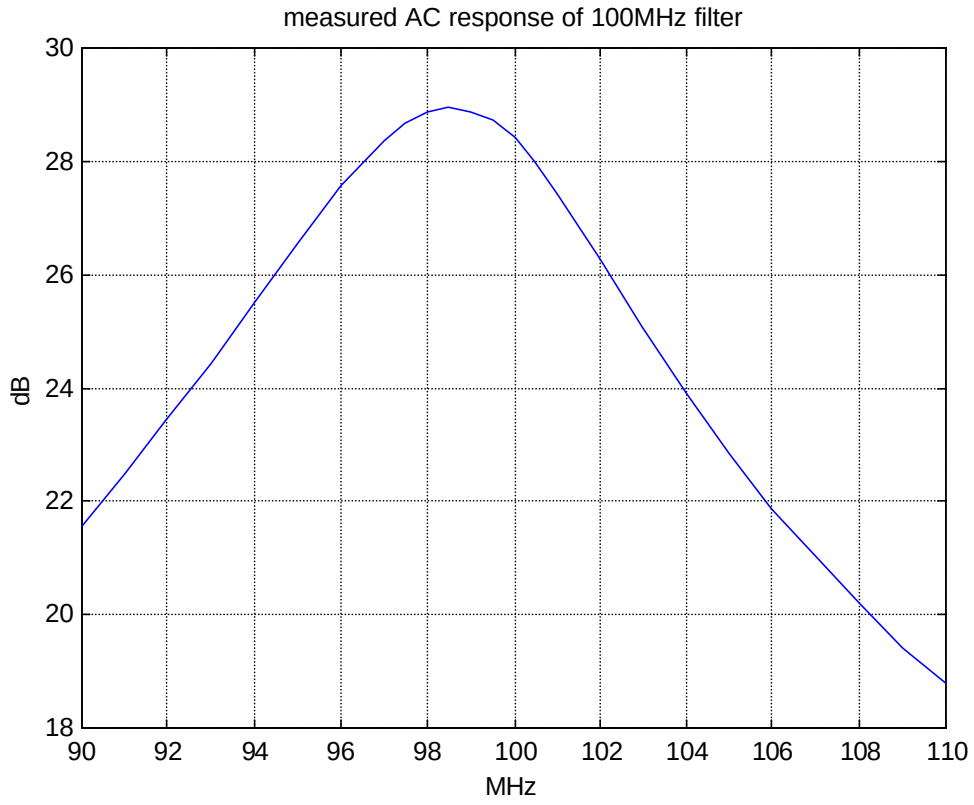


Figure B-2 AC responses obtained through transient analysis

Characteristic parameters of the two simulation results are extracted and compared in Table B-1.

Table B-1 Comparisons of simulation results—characteristic parameters

	Gain (dB)	Freq (MHz)	BW(MHz)	Q
Direct AC	30	100	6	16.7
Tran->AC	28.8	98.5	3.9	26

Listed in Table B-2 are detail data obtained from two simulation approaches.

Table B-2 comparisons of simulation results—gains

Frequency (MHz)	Gain obtained from AC analysis (dB)	Gain obtained from AC analysis (linear)	Gain obtained from transient analysis (dB)	Gain obtained from transient analysis (linear)	? (linear)	? (dB)
90	20.06	10.07	21.55	11.95	-1.88	-1.49
91	20.93	11.13	22.49	13.32	-2.19	-1.56
92	21.86	12.29	23.45	14.88	-2.59	-1.59
93	22.88	13.93	24.44	16.67	-2.74	-1.56
94	23.98	15.81	25.49	18.81	-3.00	-1.51
95	25.16	18.11	26.56	21.27	-3.06	-1.40
96	26.42	20.94	27.56	23.88	-2.94	-1.14
97	27.70	24.27	28.33	26.09	-1.82	-0.63
98	28.88	27.80	28.87	27.76	0.04	0.91
99	29.73	30.65	28.88	27.80	2.85	0.85
100	30.00	31.62	28.41	26.34	5.28	1.59
101	29.59	30.16	27.44	23.56	6.6	2.15
102	28.70	27.23	26.26	20.56	6.67	2.44
103	27.57	23.91	25.06	17.91	6.00	2.51
104	26.28	20.61	23.91	15.68	4.93	2.37
105	25.14	18.07	22.82	13.84	5.03	2.32
106	24.11	16.05	21.88	12.42	3.63	2.23
107	23.15	14.37	21.02	11.24	3.13	2.13
108	22.25	12.96	20.21	10.24	2.72	2.04
109	21.42	11.78	19.42	9.35	2.43	2.00
110	20.65	10.78	18.81	8.72	2.06	1.84

We can see that the two simulation approaches yield different results. Difference of center frequencies is 1.5MHz, 1.5% of the desired value of 100MHz. There are more than 50% difference in the 3-dB bandwidth, and about a 40% difference in Q. Observe from table II that the difference between gains at the same frequency varies from around half dB to more than 2dB. Shown in Figure B-3 are differences between the AC responses obtained by the two approaches.

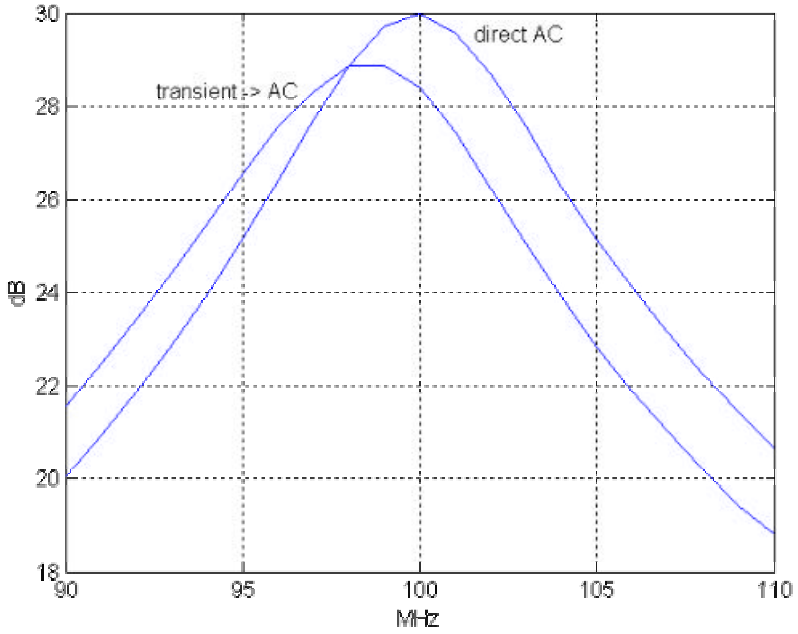


Figure B-3 Comparison of simulation results

To validate simulation results, and show that nonlinearity of the active devices was not the cause of the discrepancy, a high Q bandpass test circuit is built using ideal passive RLC components (Figure B-4).

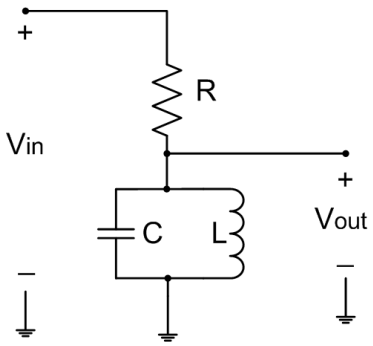


Figure B-4 a bandpass filter built using ideal RLC

Transfer function of the circuit shown in Figure A-4 is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s\frac{1}{RC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}}$$

Choose $R = 2K\Omega$, $L = 101nH$, and $C = 25pF$, simulation results obtained from AC analysis is shown in Figure B-5.

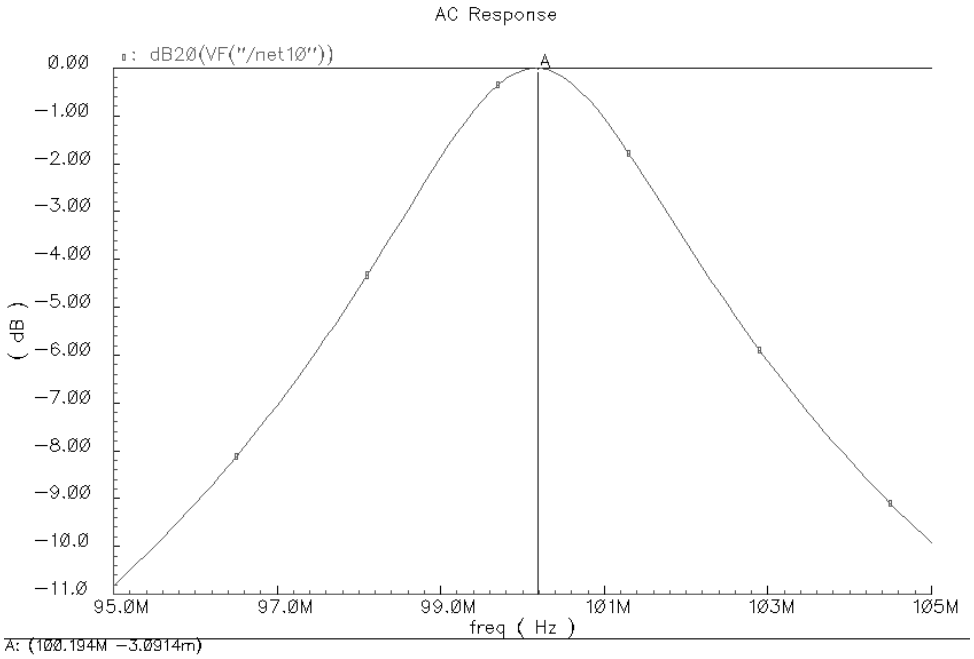


Figure B-5 Results of AC analysis of circuit in Figure 4

Figure B-5 shows that the center frequency of the bandpass filter is 100.19MHz and the mid-band loss is 0.003 dB. Figure B-6 shows a comparison of AC response results obtained using two approaches. Plotted in dotted line is the ac response obtained through transient analysis, and plotted in solid line are the results obtained from AC analysis. From the dotted plot, we can see that the center frequency is 99.9MHz, and mid-band loss is 0.084 dB.

Theoretical analysis shows that:

$$f_0 = \frac{1}{2p\sqrt{LC}} = \frac{1}{2 \times 3.14 \times \sqrt{101 \times 10^{-9} \times 25 \times 10^{-12}}} = 100.16MHz$$

Mid-band loss = 0dB

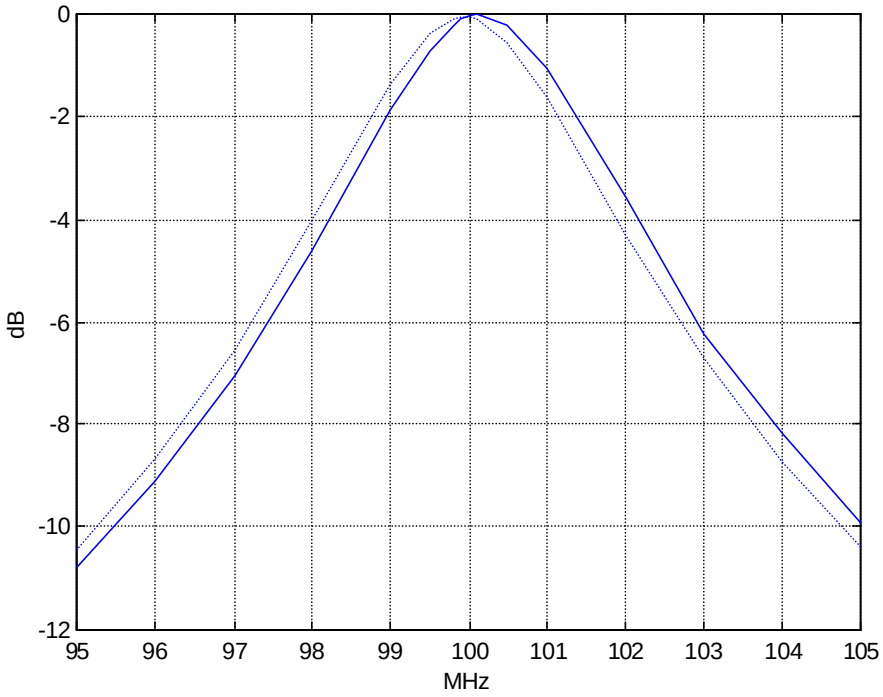


Figure B-6 Comparison of simulation results

Table B-3 shows a comparison of characteristic parameters extracted from two curves in Figure B-6 and theoretical analysis.

Table B-3 Comparison of simulation and theoretical analysis results

	Frequency (MHz)	3-dB bandwidth (MHz)	Q	Mid-band loss (dB)
AC analysis	101.19	3.18	31.82	0.003
Transient analysis	99.90	3.17	31.51	0.084
Theoretical	101.16	3.21	31.47	0

Conclusions:

- Both analyses yield correct bandpass shape curves. In other words, both analyses yields correct results at zero or infinite frequencies.
- Simulation results obtained from AC analysis agree with theoretical calculations when all circuit components are ideally linear and noiseless.
- Simulation results obtained through transient analysis might not be accurate due to convergence issues including controls and setups.
- Considering nonlinear circuit elements, transient analysis results in smaller gain compared to AC analysis at peak frequencies. This is due to loss through high order harmonics.

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